HIGH-SPEED AND LOW-POWER PROGRAMMABLE FREQUENCY DIVIDER

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ABSTRACT

This paper presents a novel 2/3 divider cell circuit design for a truly modular programmable frequency divider with high-speed, low-power, and high input-sensitivity features. In this paper, the proposed flip-flop based 2/3 divider cell adopts dynamic E-TSPC circuit that not only reduces power consumption, but also improves operation speed and input sensitivity. The whole design was implemented using the TSMC 0.18 μm 1P6M CMOS process. With an 8-stage 2/3 divider cell, the measurement results indicate that the proposed circuit operates up to 5.8GHz with the power-consumption less than 3.24mW.

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1. INTRODUCTION

One of the most critical blocks in phase-locked loops (PLLs) is the frequency divider. The key design issues of the frequency divider include high speed, low power, high input sensitivity, and high reusability. The operating frequency of PLL is limited by the frequency divider and voltage-controlled oscillator (VCO). In order to process the high output frequency of VCO, a high speed frequency divider causes the PLL to result in high power dissipation which can be as much as 50 % of the entire PLL [1]. With high input sensitivity, the divider can also reduce the output power of VCO buffer thus the power dissipation of the PLL. In addition, a divider with wider frequency range not only easily meets the required VCO frequency range, but tolerates the process-voltage-temperature (PVT) variations. Finally, the use of modular divider cells makes the divider to be reusability to reduce design complexity (duty time).

The most popular programmable frequency divider for high frequency applications is the truly modular frequency divider [1-5] because of its local reloading scheme. In the programmable divider, the 2/3 divider cell is implemented using Current-Mode Logic (CML) for high speed operation at cost of high power consumption. Moreover, the CML technique requires a certain amount of resistor and bias current resulting in high cost and design complexity due to PVT variations. In addition, low supply voltage of deep sub-micron circuits makes the CML technique inefficient for high-speed circuit design because of the headroom issue.

The advantage of Extended True-Single-Phase-Clock (E-TSPC) Flip-Flop over the more traditional CML logic in terms of power consumption and input sensitivity are due to the reduced parasitic capacitive loads [6]. In the conventional latch-based 2/3 divider cell design, the E-TSPC Flip-Flop can be used to perform two CML latch functions [7], however, due to an output node and an AND gate are located between two latches in the End-of-Cycle logic part of the conventional latch-based 2/3 divider cell, an output node and an AND function must be located in the internal node of E-TSPC that requires large transistor size for high speed consideration, thus results in high power consumption. In order to replace the CML latch with E-TSPC Flip-Flop, the conventional latch based 2/3 divider cell must be modified to Flip-Flop based 2/3 divider cell.

This work proposes a Flip-Flop based 2/3 divider cell with E-TSPC for a high-speed, low-power, high input sensitivity, low phase noise and wide frequency range. An 8-stage truly modular programmable divider using the proposed 2/3 cell is implemented in TSMC 0.18 μm CMOS technology with a supply voltage of 1.8 V. The measurement results show that a 5.8 GHz, 3.24 mW programmable divider is achieved with very small active area, (100 μm × 20 μm). With input power of -20dBm, the divider has a wide operation range up to 4GHz.

2. THE TRULY MODULAR PROGRAMMABLE DIVIDER

Figure 1 shows the truly modular programmable divider with conventional latch based 2/3 divider cell. The 2/3 divider cell takes three input signals FI, MI, and P, and produces two output signals MO and FO. For the divide-by-2 mode, the mode select signal MS is 1 resulting that FO=FI/2. For the divider-by-3 mode, the signals P=1, Q=1, MI=1, and FI=0 before passing the dash line E_A. The rising edge of FI at dash line E_A causes that MO is changed from 0 to 1, and then the falling edge of FI at dash line E_B causes that MS is changed from 1 to 0. As a result, FO=FI/3.

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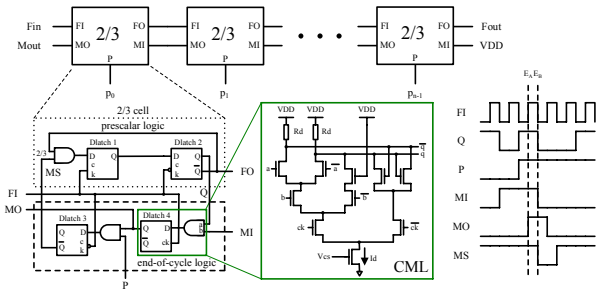

Fig. 1. The conventional 2/3 divider cell and timing diagram.

Figure 2 shows the proposed Flip-Flop based 2/3 divider cell with E-TSPC Flip-Flop circuitry. The circuit consists of two Flip-Flops with AND gate function, two INV gates, and one NAND gate. The proposed 2/3 divider cell takes three input signals FI, MI, and P, and produces two output signals MO and FO. For the divide-by-2 mode (P=0 or MO=0), the mode select signal MS is 1 resulting that FO=FI/2. For the divider-by-3 mode, the signals P=1, FO=1, MI=1, and FI=1 before passing the line E_C. The falling edge of FI at dash line E_C causes that MO is changed from 0 to 1 that causes MS is changed from 1 to 0. As a result, FO=FI/3. Therefore, the behavior of the proposed Flip-Flop based 2/3 divider cell is equal to the conventional one.

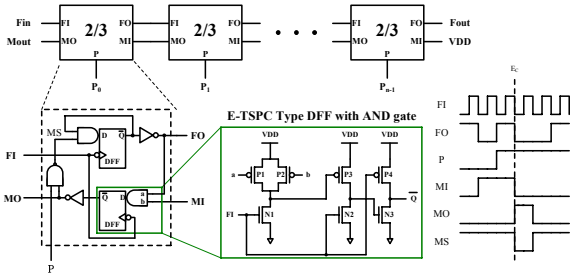

Fig. 2. The proposed 2/3 divider cell and timing diagram.

3. THE PROPOSED 2/3 DIVIDER CELL STRUCTURE

The divider cell can be realized by either the static flip-flops (ST-FFs) or dynamic FFs (DY-FFs). The power consumption of ST-FFs is proportional to its operation frequency. The aspect ratios (W/L) of the transistors employed in DY-FFs determine its power consumption and operation speed. As far as the power efficiency is concerned, the DY-FFs may be used for high speed operation, while ST-FFs for low speed operation. Therefore, to develop a programmable divider which achieves better Fin,max, the E-TSPC-type DY-FFs was selected in our circuit design.

Low power dissipation is also one of our major concerns for selecting the size of FFs. In general, the first stage of the multi-stage programmable divider using (2/3) divider cells consumes approximately 50% power of the entire divider because it takes the maximum input frequency (Fin,max) of the divider. Similarly, the second stage handles (1/2)Fin,max and consumes approximately 25% of the total power of the divider. Therefore, to develop a programmable divider which achieves lower power consumption, the transistors in the first stage required larger aspect ratios, i.e., W=1.83 µm, 1.36 µm, 0.70 µm, and 2.30 µm for transistors P1(=P2=P4), P3, N1, and N2(=N3), respectively; The transistor sizes in the second stage are smaller, i.e., W=0.89 µm, 0.42 µm, 0.22 µm, and 0.89 µm for P1(=P2), P3(=P4), N1, and N2(=N3), respectively. Since the later stages have smaller Fin,max, their transistor sizes can be reduced accordingly. However, to reduce our design efforts, we take the smaller transistor sizes for Stages #3 to #8.

4. MEASUREMENT RESULTS

The proposed divider using 8 stages of dynamic-type 2/3 divider cells with input buffer has been implemented in TSMC 0.18mm CMOS process with 1.8V supply voltage, as shown in Fig. 3, where its core area is 100µm × 20µm. Measured result in Fig. 4 shows that the phase noise at the frequency offsets of 1KHz and 1MHz are -112dBc/Hz and -137dBc/Hz, respectively, where the divider is operated at 5.8GHz with the modulus of 511. The low phase noise is due to the use of E-TSPC circuit which can be scaled well with the advanced processes.

Fig. 5 shows the measured waveforms for the division operations with the modulus of 511, where the input power is -2dBm and the input frequency is 5.8GHz. Fig. 6 shows the input power sensitivity for various operating frequencies up to 5.8GHz. Results show that the divider can be fully operated with an input power of 1dBm in this wide range. Even with a very low input power of -20dBm, the divider still has a wide operation range up to 4GHz.

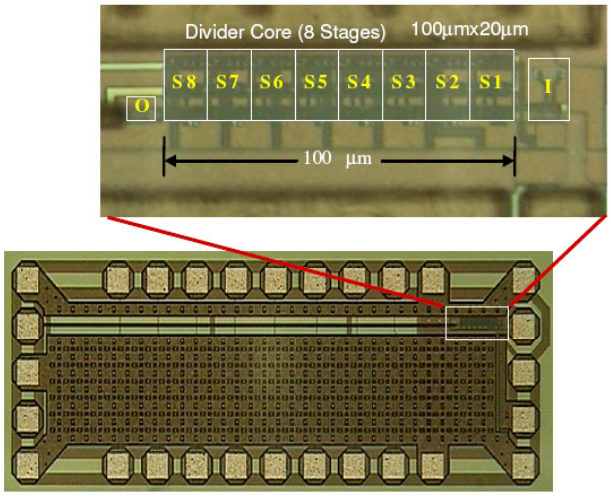

Fig. 3. The die photo of the proposed frequency divider.

Fig. 4. Measured phase noise of the frequency divider at Fin = 5.8GHz and modulus = 511.

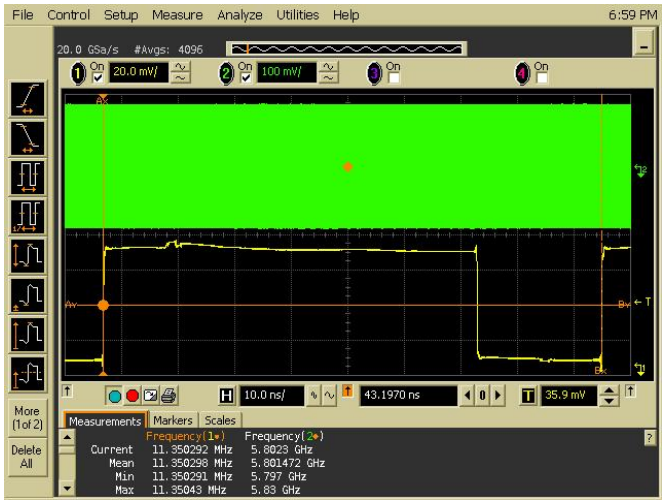

Fig. 5. Measured output waveform of the frequency divider at Fin = 5.8GHz and modulus = 511.

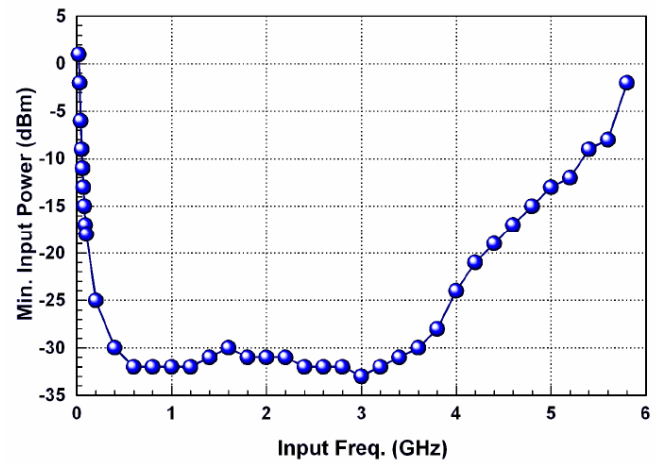

Fig. 6. Measured input sensitivity of the frequency divider.

Fig. 7 plots the operating frequency, power consumption, and power efficiency at various supply voltages ranged from 0.8 V to 2.6 V. Results show, at a supply voltage of 1.8 V, the maximum input frequency and power consumption are 5.8GHz and 3.24mW, respectively. Note that the dynamic-type E-TSPC has the inherent low power capability than CML structure. Therefore, the power efficiency is 1.79GHz/mW. Results also show that, if a supply voltage of 0.8V is applied to the proposed divider, a power efficiency of 5.4GHz/mW can be achieved.

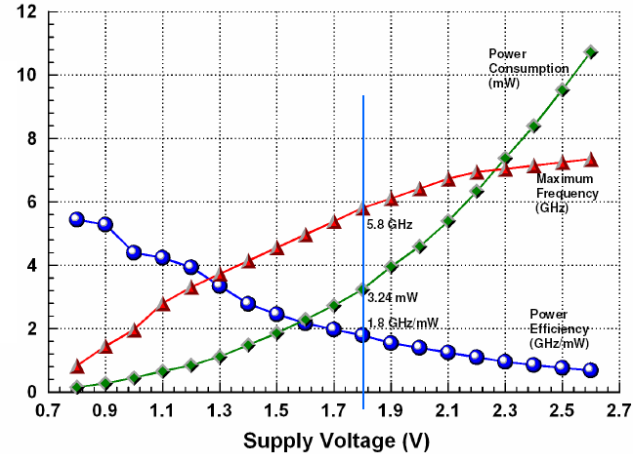

Fig. 7. Measured results of the frequency divider.

Table I compares the performance of existing frequency dividers. The proposed divider achieves the best performance of power efficiency. In order to demonstrate the low power and high operating frequency of the proposed divider, a test chip of frequency synthesizer has been implemented in TSMC 0.18µm CMOS process with 1.8V supply voltage. The major components of the PLL include a ring type VCO, an edge-missing compensator (EMC) [9], and the proposed programmable frequency divider (DIV).

Table I. Comparison table.

	[2]	[6]	[3]	[8]	[5]	[1]	This work
Tech. (nm)	350	250	180	180	90	90	180
VDD (V)	2.2	2.5	2	1.8	1.2	0.65	1.8
Fin, Max (GHz)	N/A	5.7	3.5	1.8	4.7	2.5	5.8
Power (mW)	N/A	6.25	22	5.8	2.76	3.5	3.24
Power Eff. (GHz/mW)	0.77	0.91	0.16	0.31	1.7	0.71	1.79

Fig. 8 shows the die photo of the major components and the measured data for the PLL. Results show that, with the operating frequency ranged between 1.9GHz and 3.7GHz, and the total power consumption of the PLL is about 20.6mW. Fig. 9 shows the performance of phase noises are -85.89, -88.31, -81.59, and -90.03 dBc/Hz for the frequency offsets of 1k, 10k, 100k, and 1M Hz, respectively.

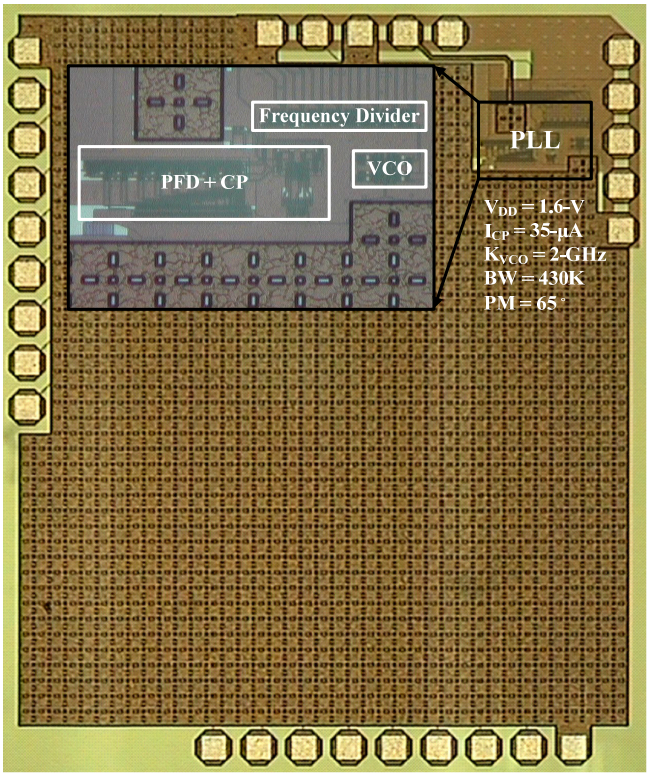

Fig. 8. The die photo of testing PLL.

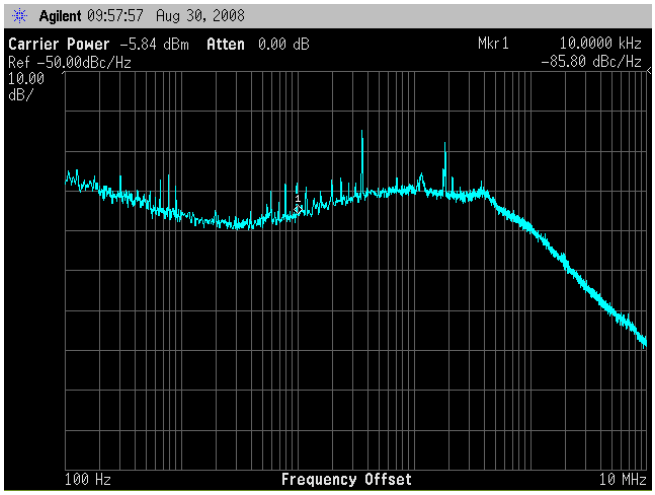

Fig. 9. The measured phase noise of testing PLL.

5. CONCLUSIONS

In this paper, a high-speed, low-power, and high-sensitivity circuit design for truly modular programmable frequency divider has been proposed. Based on the flip-flop based 2/3 divider cell design, the circuit achieve high speed and low power features by using E-TSPC structure. The measurement results showed that the operation speed of the chip achieves 5.8GHz at 1.8 V. Moreover, the experimental results indicate that the minimum operating voltage of this chip is scaled down to 0.8 V. The power-efficient of the circuit is up to 1.79 GHz/mW. This circuit is appropriate for high speed and low-power design and is suitable to be embedded in its applications.

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