

# An Analytical Investigation on the Charge Distribution and Gate Control in the Normally-Off GaN Double-Channel MOS-HEMT

Jin Wei<sup>1</sup>, Member, IEEE, Meng Zhang<sup>1</sup>, Baikui Li, Member, IEEE, Xi Tang<sup>1</sup>, Student Member, IEEE, and Kevin J. Chen<sup>1</sup>, Fellow, IEEE

**Abstract**—A systematic analytical investigation of the charge distribution and gate control of the normally-off GaN double-channel MOS-HEMT (DC-MOS-HEMT) is presented in this paper. Compared to conventional GaN MOS-HEMT, the DC-MOS-HEMT features a thin AlN insertion layer (AlN-ISL) below the original two dimensional electron gas (2DEG) channel, thus forming a second channel at the interface between AlN-ISL and the underlying GaN. This paper reveals the impact of the AlN-ISL on the 2DEG distribution and the gate control of the channels. The sensitivity of  $V_{th}$  against the recess depth is also analytically studied and is found to be nearly independent of the recess depth as long as the recess is terminated in the upper channel layer. The analytical results are well supported by numerical device simulations, and the physical mechanisms behind these findings are explained along with the analytical investigations.

**Index Terms**—Analytical, charge control, double-channel MOS-HEMT (DC-MOS-HEMT), gate recess, normally-off.

## I. INTRODUCTION

MOS-HEMTs with partially or fully recessed gate are considered as a promising solution for normally-off GaN power transistors because the MOS-gate is compatible with the mainstream gate driver ICs [1]–[3]. The partially recessed gate preserves the high-mobility heterojunction underneath the gate, thus maintaining a low

Manuscript received January 22, 2018; revised March 30, 2018; accepted April 23, 2018. This work was supported in part by the Guangdong Science and Technology Department under Grant 2017B010113002 and in part by the Shenzhen Science and Technology Innovation Commission under Grant JCYJ20160229205511222. The review of this paper was arranged by Editor B. Iñiguez. (J. Wei and M. Zhang contributed equally to this work.) (Corresponding author: Kevin J. Chen.)

J. Wei and X. Tang are with the HKUST Shenzhen Research Institute, Shenzhen 518000, China, and also with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: jwei@connect.ust.hk; xtang@connect.ust.hk).

M. Zhang is with the Department of Industrial and Systems Engineering, The Hong Kong Polytechnic University, Hong Kong (email: sara.zhang@connect.polyu.hk).

B. Li is with the College of Optoelectronic Engineering, Shenzhen University, Shenzhen 518000, China (e-mail: libk@szu.edu.cn).

K. J. Chen is with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, and also with the HKUST Shenzhen Research Institute, Shenzhen 518000, China (e-mail: eekjchen@ust.hk).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2018.2831246

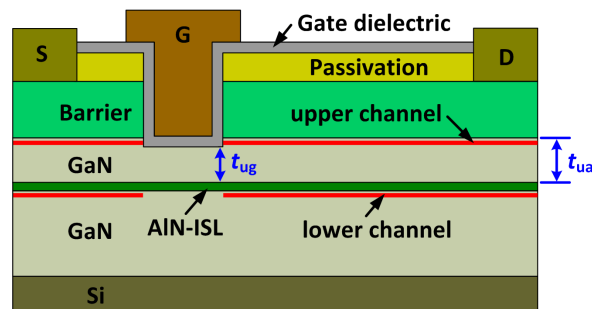


Fig. 1. Schematic cross-sectional structure of the DC-MOS-HEMT.

ON-resistance ( $R_{on}$ ). However, as the barrier layer possesses a strong polarization field, a tiny variation of the recess depth renders an appreciable change in the threshold voltage ( $V_{th}$ ), while precise control of the recess depth is rather difficult in practical fabrication. On the contrary,  $V_{th}$  of the fully recessed gate structure is much less sensitive to the recess depth, but the electron mobility in its MOS-channel is typically low, leading to a significant increase of  $R_{on}$  [4]. A recently reported double-channel MOS-HEMT (DC-MOS-HEMT) solves the above dilemma with a thin AlN insertion layer (AlN-ISL) beneath of original 2DEG channel to form a second channel [5], [6]. The cross-sectional structure of the DC-MOS-HEMT is shown in Fig. 1. The gate recess is terminated at the upper GaN channel layer.  $V_{th}$  of the DC-MOS-HEMT is insensitive to the recess depth since the energy band is nearly flat in the upper GaN channel layer before the device is turned on [6], [7]. A low  $R_{on}$  is obtained by coupling two channels at access region to the high-mobility lower channel at the gate region [5], [8]. Based on the unique properties of the DC-MOS-HEMT, a double-channel SBD [9] and a DC-MOS-HEMT with integrated freewheeling diode [10] were also demonstrated.

To release the full potential of the DC-MOS-HEMT, it is of value to develop analytical modeling of the device, since it provides physical insights of operating mechanism and serves as a guidance for device design. Although analytical modeling on the charge distribution and gate control in GaN single-channel HEMTs has been well established [11]–[14], the analytical study on the DC-MOS-HEMT has not been reported. In this paper, a systematic analytical investigation

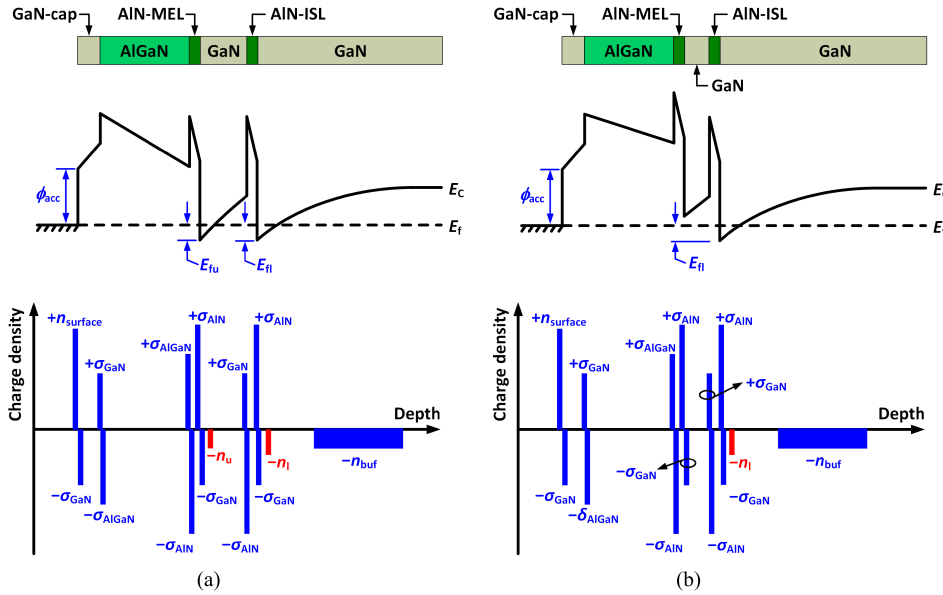


Fig. 2. Schematic conduction band diagrams and charge distributions at the access region of the DC-MOS-HEMT. The surface barrier  $\phi_{acc}$  is determined by where the Fermi level is pinned. For an ungated region, this is determined by the surface/interface states.  $n_{surface}$  is the density of ionized surface/interface traps. There is a critical thickness of the upper channel layer  $t_{ua-crit}$ . (a) When  $t_{ua} > t_{ua-crit}$ , two channels exist. (b) When  $t_{ua} \leq t_{ua-crit}$ , only the lower channel is formed.

is performed on the DC-MOS-HEMT. The main feature for the double-channel heterostructure is the presence of the AlN-ISL. Therefore, the impact of the AlN-ISL is highlighted. In Section II, the charge distribution in the access region will be investigated. Section III will present the gate control of the two channels underneath. The main factors influencing the threshold voltages of each channel will be identified. Conclusions will be drawn in Section IV.

## II. CHARGE DISTRIBUTION AT THE ACCESS REGION

As shown in Fig. 1, the double-channel heterostructure consists of a barrier layer, a GaN upper channel layer, an AlN-ISL, and a GaN buffer/transition layer on a silicon substrate. The barrier layer further consists of a GaN cap layer, an AlGaN layer, and an AlN mobility enhancement layer (AlN-MEL). The main parameters used in this paper are listed in Table I. Default values are assigned to the parameters according to the devices fabricated in our previous experiments [5], [6]. The thicknesses of the upper channel layer in the access region ( $t_{ua}$ ) and in the gated region ( $t_{ug}$ ) are variables.

Figure 2 illustrates the band diagram at the access region of the DC-MOS-HEMT in equilibrium and the corresponding charge distribution. For each layer, a positive and a negative sheet charges are located at its opposite surfaces due to the polarization effects. The values of these polarization charges are calculated according to [14]. Deep into the GaN buffer layer, the electric field is assumed to be 0. A compensation doping (i.e., C-doping) is typically utilized in the buffer layer to introduce deep traps and thus to reduce the buffer leakage [15]. Ionization of these trapping states results in a space charge region. The density of the space charges ( $n_{buf}$ ) is determined by the energy level and spatial distribution

TABLE I  
LIST OF MAIN PARAMETERS IN THIS PAPER

Symbol	Quantity	Value
$t_{AIN-ISL}$	thickness of AlN-ISL	1.5 nm
$t_{ua}$	thick. of upper channel at access region	variable
$t_{ug}$	thick. of upper channel at gate region	variable
$t_{AIN-MEL}$	thickness of AlN-MEL	1.5 nm
$t_{AlGaN}$	thickness of AlGaN barrier	17 nm
$x_{AlGaN}$	Al composition in AlGaN barrier	0.25
$t_{GaN-cap}$	thickness of GaN cap	3 nm
$t_{Al_2O_3}$	thickness of $Al_2O_3$ gate dielectric	18 nm
$n_{buf}$	density of space charge in the buffer	$0.6 \times 10^{12} \text{ cm}^{-2}$
$n_{it}$	density of effective interface charges	$1.5 \times 10^{13} \text{ cm}^{-2}$ <sup>a</sup>
$\phi_{acc}$	surface barrier height at access region	0.7 eV
$\phi_G$	surface barrier height at gated region	3.47 eV

<sup>a</sup> Used unless specified otherwise

of the trapping states [16]. In this paper, we assume an acceptor trap at  $E_V + 543 \text{ meV}$  with a concentration of  $4 \times 10^{16} \text{ cm}^{-3}$ , and a donor trap at  $E_C - 616 \text{ meV}$  with a concentration of  $2 \times 10^{16} \text{ cm}^{-3}$  in the buffer layer except for the top 100 nm [17]. From electrostatic analysis and by numerical calculation, a space charge of  $n_{buf} = \sim 0.6 \times 10^{12} \text{ cm}^{-2}$  is located beneath the 2DEG channels. This space charge density is small compared to the polarization charges and the 2DEG. The surface barrier height ( $\phi_{acc}$ ) is determined by where the Fermi level is pinned, which is strongly process dependent [18]. In this paper,  $\phi_{acc} = 0.7 \text{ eV}$  is assumed.

### A. Analytical Expressions in Double-Channel Heterostructures

When  $t_{ua}$  is larger than a critical thickness  $t_{ua-crit}$  (as will be determined in Section II-B), two channels exist in the

heterostructure. The conduction band diagram and the charge distribution are illustrated in Fig. 2(a) for this case. The Fermi energies  $E_{fl}$  and  $E_{fu}$  are defined as the energy differences between the Fermi level and the conduction band minimum at the lower and upper channels, respectively; and they are functions of the 2DEG density in the lower channel ( $n_l$ ) and that in the upper channel ( $n_u$ ) [13], [14]

$$E_{fl} = \left( \frac{9q^2\pi\hbar n_l}{8\epsilon_{GaN}\sqrt{8m_{GaN}^*}} \right)^{2/3} + \frac{\pi\hbar^2 n_l}{m_{GaN}^*} \quad (1)$$

$$E_{fu} = \left( \frac{9q^2\pi\hbar n_u}{8\epsilon_{GaN}\sqrt{8m_{GaN}^*}} \right)^{2/3} + \frac{\pi\hbar^2 n_u}{m_{GaN}^*}. \quad (2)$$

At equilibrium, the Fermi level is flat along the depth of the heterostructure. Applying Gauss's Law from the lower channel to the upper channel, we obtain

$$-E_{fl} + \Delta E_{C-AIN/GaN} + \frac{q^2(\sigma_{AIN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} - \Delta E_{C-AIN/GaN} + \frac{q^2(-n_l - n_{buf})}{\epsilon_{GaN}} \cdot t_{ua} + E_{fu} = 0$$

Simplifying the above equation,  $n_l$  is obtained

$$n_l = \left[ \frac{q^2(\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} + E_{fu} - E_{fl} \right] / \left( q^2 \frac{t_{ua}}{\epsilon_{GaN}} + q^2 \frac{t_{AIN-ISL}}{\epsilon_{AIN}} \right) - n_{buf}. \quad (3)$$

Similarly, Gauss's Law is applied from the upper channel to the surface of the GaN cap layer

$$-E_{fu} + \Delta E_{C-AIN/GaN} + \frac{q^2(\sigma_{AIN} - \sigma_{GaN} - n_l - n_u - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-MEL} - \Delta E_{C-AIN/AIGaN} + \frac{q^2(\sigma_{AIGaN} - \sigma_{GaN} - n_l - n_u - n_{buf})}{\epsilon_{AIGaN}} \cdot t_{AIGaN} - \Delta E_{C-AIGaN/GaN} + \frac{q^2(-n_l - n_u - n_{buf})}{\epsilon_{GaN}} \cdot t_{GaN-cap} - \phi_{acc} = 0.$$

Rearranging the above equation,  $n_u$  is expressed as

$$n_u = \left[ \frac{q^2(\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \cdot t_{AIN-MEL} + \frac{q^2(\sigma_{AIGaN} - \sigma_{GaN})}{\epsilon_{AIGaN}} \cdot t_{AIGaN} - E_{fu} - \phi_{acc} \right] / \left( q^2 \frac{t_{AIN-MEL}}{\epsilon_{AIN}} + q^2 \frac{t_{AIGaN}}{\epsilon_{AIGaN}} + q^2 \frac{t_{GaN-cap}}{\epsilon_{GaN}} \right) - n_l - n_{buf}. \quad (4)$$

### B. Critical Thickness for the Upper Channel

From (3) and (4),  $n_t (= n_l + n_u)$  is independent on  $t_{ua}$ , while a smaller  $t_{ua}$  allocates more electrons to the lower channel. When  $t_{ua}$  decreases to a critical value  $t_{ua-crit}$ , the 2DEG in the upper channel vanishes, and only the lower channel exists.

Therefore, when  $t_{ua} = t_{ua-crit}$ , we have  $n_u = 0$  and  $E_{fu} = 0$ . From (4), the 2DEG density in the lower channel is

$$n_l = \left[ \frac{q^2(\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \cdot t_{AIN-MEL} + \frac{q^2(\sigma_{AIGaN} - \sigma_{GaN})}{\epsilon_{AIGaN}} \cdot t_{AIGaN} - \phi_{acc} \right] / \left( q^2 \frac{t_{AIN-MEL}}{\epsilon_{AIN}} + q^2 \frac{t_{AIGaN}}{\epsilon_{AIGaN}} + q^2 \frac{t_{GaN-cap}}{\epsilon_{GaN}} \right) - n_{buf}. \quad (5)$$

After obtaining  $n_l$ ,  $t_{ua-crit}$  can be expressed in terms of  $n_l$ . Rearranging (3), we obtain

$$t_{ua-crit} = \frac{\epsilon_{GaN}}{q^2(n_l + n_{buf})} \cdot \left[ \frac{q^2(\sigma_{AIN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} - E_{fl} \right]. \quad (6)$$

From (6),  $t_{ua-crit}$  is 2.7 nm using the parameters from Table I.

### C. 2DEG Density When Only Lower Channel Exists

For  $t_{ua} < t_{ua-crit}$ , expressions (3) and (4) are not valid. The conduction band diagram and the charge distribution are illustrated in Fig. 2(b) for this case when only the lower channel exists. By applying Gauss' Law from the lower channel to the surface of the cap layer, the electrostatic equation is obtained

$$-E_{fl} + \Delta E_{C-AIN/GaN} + \frac{q^2(\sigma_{AIN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} - \Delta E_{C-AIN/GaN} + \frac{q^2(-n_l - n_{buf})}{\epsilon_{GaN}} \cdot t_{ua} + \Delta E_{C-AIN/GaN} + \frac{q^2(\sigma_{AIN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-MEL} - \Delta E_{C-AIN/AIGaN} + \frac{q^2(\sigma_{AIGaN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIGaN}} \cdot t_{AIGaN} - \Delta E_{C-AIGaN/GaN} + \frac{q^2(-n_l - n_{buf})}{\epsilon_{GaN}} \cdot t_{GaN-cap} - \phi_{acc} = 0.$$

Simplifying the above equation,  $n_l$  is obtained

$$n_l = \left[ \frac{q^2(\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} + \frac{q^2(\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \cdot t_{AIN-MEL} + \frac{q^2(\sigma_{AIGaN} - \sigma_{GaN})}{\epsilon_{AIGaN}} \cdot t_{AIGaN} - E_{fl} - \phi_{acc} \right] / \left( q^2 \frac{t_{AIN-ISL}}{\epsilon_{AIN}} + q^2 \frac{t_{ua}}{\epsilon_{GaN}} + q^2 \frac{t_{AIN-MEL}}{\epsilon_{AIN}} + q^2 \frac{t_{AIGaN}}{\epsilon_{AIGaN}} + q^2 \frac{t_{GaN-cap}}{\epsilon_{GaN}} \right) - n_{buf}. \quad (7)$$

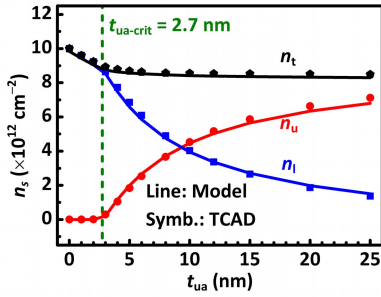


Fig. 3. 2DEG densities in the access region of the DC-MOS-HEMT by analytical modeling and TCAD numerical simulation.  $n_t = n_u + n_l$ .

#### D. Discussion on 2DEG Distribution

According to (7), the location of the AlN-ISL has a significant impact upon the 2DEG distribution, as shown in Fig. 3. When  $t_{ua} \leq t_{ua-crit}$ ,  $n_u = 0$ , and  $n_l$  is calculated using (7); while for  $t_{ua} \geq t_{ua-crit}$ , (3) and (4) are used for calculation of  $n_l$  and  $n_u$ . The numerical results agree very well with the analytical results, which validates the analytical modeling.

The AlN-ISL introduces a charge dipole into the heterostructure. The negative charge at the upper surface of the AlN-ISL reduces the 2DEG density in the upper channel, and this is compensated by an increase of 2DEG density in the lower channel. According to (3), (4), and (7), a large percentage of electrons are located in the lower channel when the AlN-ISL is close to the upper channel. As the separation between the AlN-ISL and the upper channel ( $t_{ug}$ ) is enlarged, more electrons are allocated to the upper channel.

The total 2DEG density of the two channels ( $n_t$ ) stays almost a constant when  $t_{ua} > t_{ua-crit}$ , which agrees with (4). However, when  $t_{ua} < t_{ua-crit}$ ,  $n_t$  becomes a much stronger function of  $t_{ua}$ , as expected from (7). From an aspect of electrostatics, this is easy to understand. The net charges along the depth of the heterostructure are zero. The change in  $n_t$  mainly originates from the change in the ionization of surface traps. With only the lower channel existing, the dipole in the AlN-ISL causes more surface traps to be ionized, and an equal increase of electrons in the lower channel to compensate the change of surface charges.  $n_t$  is thus increased. When the upper channel is formed, the Fermi level at the upper channel is pinned near the conduction band. Therefore, the ionization rate of the surface traps is unaffected owing to the screening effect of the upper channel, resulting in a nearly constant  $n_t$ .

### III. CHARGE DISTRIBUTION AT THE GATED REGION

#### A. 2DEG Density When Both Channels Turned On

The band diagram and charge distribution at the gated region are illustrated in Fig. 4. An effective net positive charge ( $n_{it}$ ) is typically present at the MOS interface [19], [20], which may contain fixed charges, ionized traps, and charges in the bulk of the dielectric. The dielectric bulk charges can be modeled as an interface charge with equivalent impact upon the gate control [21]. In this section, we assume  $n_{it} = 1.5 \times 10^{13} \text{ cm}^{-2}$ , which fits the fabricated device as will be discussed later.

When  $V_G$  is greater than  $V_{th-u}$  (the threshold voltage of the upper channel, as will be determined in Section III-B), both channels are turned on. Similar to the procedure used in

Section II, we apply Gauss' Law from the lower channel to the upper channel. After rearranging the equation, the 2DEG density in the lower channel  $n_l$  is obtained in (8), which is the same as (3)

$$n_l = \left[ \frac{q^2 (\sigma_{\text{AlN}} - \sigma_{\text{GaN}})}{\epsilon_{\text{AlN}}} \cdot t_{\text{AlN-ISL}} + E_{fu} - E_{fl} \right] / \left( q^2 \frac{t_{ug}}{\epsilon_{\text{GaN}}} + q^2 \frac{t_{\text{AlN-ISL}}}{\epsilon_{\text{AlN}}} \right) - n_{\text{buf}}. \quad (8)$$

To achieve the expression for the 2DEG density in the upper channel, we apply Gauss' Law from the upper channel to the gate electrode

$$-E_{fu} + \Delta E_{C-\text{Al}_2\text{O}_3/\text{GaN}} + \frac{q^2 (n_{it} - \sigma_{\text{GaN}} - n_l - n_u - n_{\text{buf}})}{\epsilon_{\text{Al}_2\text{O}_3}} \cdot t_{\text{Al}_2\text{O}_3} - \phi_G + qV_G = 0.$$

Here,  $\Delta E_{C-\text{Al}_2\text{O}_3/\text{GaN}}$  is the conduction band offset, which is 2.57 eV. The 2DEG density in the upper channel is obtained by simplifying the above equation

$$n_u = \left[ \Delta E_{C-\text{Al}_2\text{O}_3/\text{GaN}} + \frac{q^2 (n_{it} - \sigma_{\text{GaN}})}{\epsilon_{\text{Al}_2\text{O}_3}} \cdot t_{\text{Al}_2\text{O}_3} - E_{fu} - \phi_G + qV_G \right] / \left( q^2 \frac{t_{\text{Al}_2\text{O}_3}}{\epsilon_{\text{Al}_2\text{O}_3}} \right) - n_l - n_{\text{buf}}. \quad (9)$$

#### B. Threshold Voltage of the Upper Channel

From (9),  $n_u$  drops as the gate voltage is decreased. When the gate voltage is decreased to  $V_{th-u}$  (the threshold voltage of the upper channel), the upper channel is turned off. At this condition,  $n_u = 0$  and  $E_{fu} = 0$ . The 2DEG density in the lower channel is obtained from (8)

$$n_l = \left[ \frac{q^2 (\sigma_{\text{AlN}} - \sigma_{\text{GaN}})}{\epsilon_{\text{AlN}}} \cdot t_{\text{AlN-ISL}} - E_{fl} \right] / \left( q^2 \frac{t_{ug}}{\epsilon_{\text{GaN}}} + q^2 \frac{t_{\text{AlN-ISL}}}{\epsilon_{\text{AlN}}} \right) - n_{\text{buf}}. \quad (10)$$

Setting  $n_u = 0$  and  $E_{fu} = 0$  in (9),  $V_{th-u}$  is determined to be

$$V_{th-u} = - \left[ \Delta E_{C-\text{Al}_2\text{O}_3/\text{GaN}} + \frac{q^2 (n_{it} - \sigma_{\text{GaN}} - n_l - n_{\text{buf}})}{\epsilon_{\text{Al}_2\text{O}_3}} \cdot t_{\text{Al}_2\text{O}_3} - \phi_G \right] / q. \quad (11)$$

#### C. 2DEG Density When Only the Lower Channel Turned On

For  $V_{th-l} < V_G < V_{th-u}$ , only the lower channel is on. Applying Gauss' Law from the lower channel to the gate

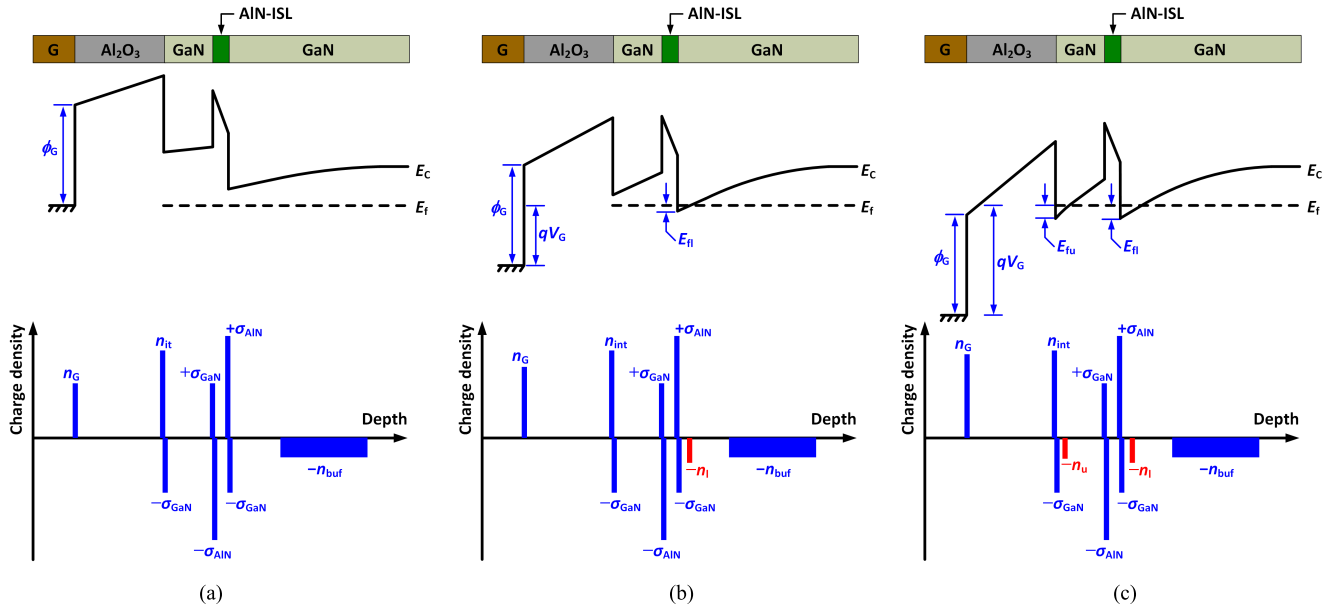


Fig. 4. Schematic band diagrams and charge distributions at the recessed gate region of the normally-off DC-MOS-HEMT. (a) When  $V_G = 0$  V, both channels are pinched off. (b) When  $V_{th-l} < V_G < V_{th-u}$ , the lower channel is turned on, but the upper channel is still off. (c) When  $V_G > V_{th-u}$ , both channels are turned on.

electrode

$$\begin{aligned}
 & -E_{fl} + \Delta E_{C-AIN/GaN} + \frac{q^2 (\sigma_{AIN} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{AIN}} \\
 & \cdot t_{AIN-ISL} - \Delta E_{C-AIN/GaN} + \frac{q^2 (-n_l - n_{buf})}{\epsilon_{GaN}} \cdot t_{ug} \\
 & + \Delta E_{C-Al2O3/GaN} + \frac{q^2 (n_{it} - \sigma_{GaN} - n_l - n_{buf})}{\epsilon_{Al2O3}} \\
 & \cdot t_{Al2O3} - \phi_G + qV_G = 0.
 \end{aligned}$$

The 2DEG density in the lower channel is obtained after simplifying the above equation

$$\begin{aligned}
 n_l = & \left[ -E_{fl} + \Delta E_{C-AIN/GaN} + \frac{q^2 (\sigma_{AIN} - \sigma_{GaN})}{\epsilon_{AIN}} \right. \\
 & \cdot t_{AIN-ISL} - \Delta E_{C-AIN/GaN} + \Delta E_{C-Al2O3/GaN} \\
 & \left. + \frac{q^2 (n_{it} - \sigma_{GaN})}{\epsilon_{Al2O3}} \cdot t_{Al2O3} - \phi_G + qV_G \right] \\
 & / \left( \frac{q^2 t_{AIN-ISL}}{\epsilon_{AIN}} + q^2 \frac{t_{ug}}{\epsilon_{GaN}} + q^2 \frac{t_{Al2O3}}{\epsilon_{Al2O3}} \right) - n_{buf}.
 \end{aligned} \quad (12)$$

#### D. Threshold Voltage of the Lower Channel

By setting  $n_l = 0$  in (12), the threshold voltage for the lower channel ( $V_{th-l}$ ) is determined as

$$\begin{aligned}
 V_{th-l} = & - \left[ \frac{q^2 (\sigma_{AIN} - \sigma_{GaN} - n_{buf})}{\epsilon_{AIN}} \cdot t_{AIN-ISL} \right. \\
 & + \frac{q^2 (-n_{buf})}{\epsilon_{GaN}} \cdot t_{ug} + \Delta E_{C-Al2O3/GaN} \\
 & \left. + \frac{q^2 (n_{it} - \sigma_{GaN} - n_{buf})}{\epsilon_{Al2O3}} \cdot t_{Al2O3} - \phi_G \right] / q.
 \end{aligned} \quad (13)$$

As the lower channel is turned on before the upper channel in the DC-MOS-HEMT,  $V_{th-l}$  is actually the threshold voltage of the device itself ( $V_{th}$ ). Therefore,

$$V_{th} = V_{th-l}. \quad (14)$$

For MOS-HEMT with a recessed gate, precise control of the recessed depth is difficult with contemporary technologies. The sensitivity of  $V_{th}$  against the recessed depth in the DC-MOS-HEMT is of significance. Differentiating (13), the  $V_{th}$  sensitivity against  $t_{ug}$  is obtained

$$dV_{th}/dt_{ug} = qn_{buf}/\epsilon_{GaN}. \quad (15)$$

The right side of (15) is the electric field in the upper channel layer originating from the space charges in the buffer.

#### E. Discussion on Gate Control

The 2DEG densities as functions of the gate voltage are plotted in Fig. 5. When  $V_G \leq V_{th-l}$ ,  $n_u = n_l = 0$ . When  $V_{th-l} \leq V_G \leq V_{th-u}$ ,  $n_u = 0$ , and  $n_l$  is calculated using (13). When  $V_G \geq V_{th-u}$ ,  $n_l$  and  $n_u$  are calculated using (8) and (9). The  $n_{it}$  value is set to fit the experimental  $V_{th}$  value (see Fig. 7) as will be discussed later. The results from analytical modeling agree well with the TCAD numerical simulation.

It is seen that the lower channel turns on first, followed by the upper channel at higher  $V_G$ . After the upper channel is turned on, the lower channel is screened from the gate voltage by the upper channel, and  $n_l$  gets saturated. The poorer saturation of  $n_l$  when  $t_{ug}$  is small is due to the strong capacitive coupling between the two channels; the small change in  $E_{fu}$  thus causes an observable effect upon  $n_l$ . The slight discrepancies of electron distribution between modeling value and simulation value when  $t_{ug} = 2$  nm, may originate



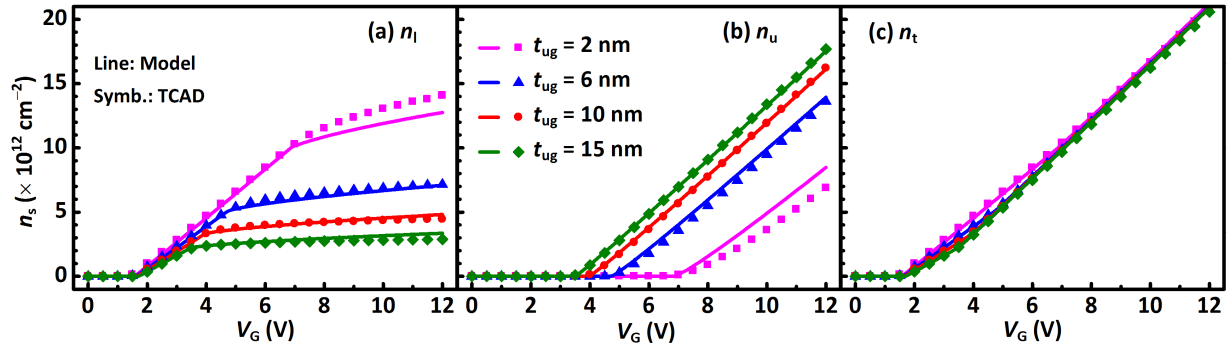


Fig. 5. 2DEG density in the gated region as functions of the gate voltage and the remaining upper channel thickness in the gated region, obtained by analytical modeling and TCAD numerical simulation. (a) 2DEG density in the lower channel. (b) 2DEG density in the upper channel. (c) Total 2DEG density.

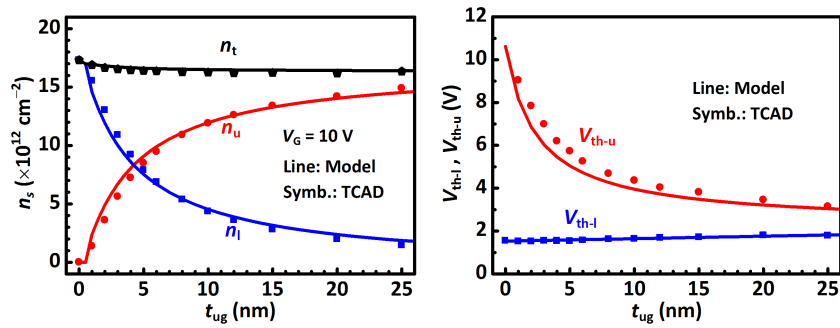


Fig. 6. (a) 2DEG densities as function of the upper channel thickness in the gated region, obtained by analytical modeling and TCAD numerical simulation. The gate voltage is fixed at 10 V. (b) Threshold voltages of the lower and upper channels as functions of  $t_{ug}$ , obtained by analytical modeling and TCAD numerical simulation.

from two factors. The quantum effect is considered in the Fermi energies in the analytical modeling process, but not considered in simulation. The 2DEG in each channel is modeled as a sheet charge with zero thickness, but it features a nonzero thickness in simulation. The influence of the two factors becomes noticeable when  $t_{ug}$  reduces to as small as 2 nm.

Figure 6(a) shows the 2DEG densities for the two channels at a fixed  $V_G$  ( $=10$  V), which is found to follow the same trend as that in the access region, as analyzed in Section III-D. A smaller  $t_{ug}$  leads to larger portion of electrons in the lower channel.

$V_{th-u}$  is a strong function of  $t_{ug}$ , as in Figs. 5(b) and 6(b). As  $t_{ug}$  decreases,  $V_{th-u}$  is pushed to higher value. Actually, the difference in  $V_{th-l}$  and  $V_{th-u}$  determines the saturated 2DEG density in the lower channel, i.e.,  $n_l \approx (V_{th-u} - V_{th-l}) \cdot C_l$ , as can be deduced from (10), (11), and (13) by approximating  $E_1 = 0$ . Here,  $C_l$  is the gate to lower channel capacitance, which is affected by  $t_{ug}$ . This agrees with the fact that smaller  $t_{ug}$  renders higher saturation 2DEG density in the lower channel. From another aspect, when  $V_G$  is fixed at  $V_{th-u}$ , the corresponding  $t_{ug}$  on the  $V_{th-u} \sim t_{ug}$  curve in Fig. 6(b) curve is the critical upper channel thickness  $t_{ug-crit}$ .

$V_{th}$  ( $= V_{th-l}$ ) is almost independent of  $t_{ug}$ , as shown in Figs. 5(a) and 6(b). As revealed by (15), this is because the electric field induced by  $n_{buf}$  is very weak, and the conduction band is nearly flat in the upper channel when  $V_{GS} = 0$  V.

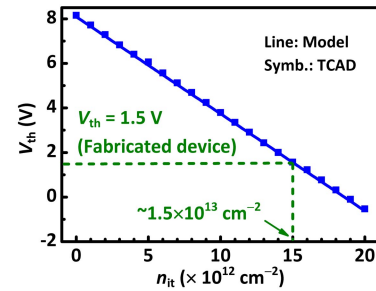


Fig. 7. Threshold voltage of DC-MOS-HEMT as a function of the effective interface charges.  $t_{ug}$  is fixed at 4.5 nm in this calculation.

The sensitivity of  $V_{th}$  against  $t_{ug}$  is a function of  $n_{buf}$ , since  $n_{buf}$  is the origin of electric field in the upper channel layer before the lower channel is turned on. With the parameters in Table I, for a 1-nm variation of recess depth,  $V_{th}$  is changed by only 12 mV. On the contrary, for conventional single channel MOS-HEMT, if the gate recess is terminated within the  $Al_{0.25}Ga_{0.75}N$  barrier layer, 1-nm variation of recess depth renders a  $\Delta V_{th}$  of  $\sim 260$  mV. When the recess is terminated within the  $AlN$ -MEL, the sensitivity of  $V_{th}$  is even higher.

The effective interface charges ( $n_{it}$ ) have an appreciable influence on  $V_{th}$  of the DC-MOS-HEMT, as shown in Fig. 7. The fabricated DC-MOS-HEMT ( $t_{ug} = 4.5$  nm) features

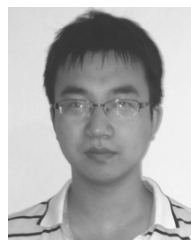
an effective  $n_{it} = 1.5 \times 10^{13} \text{ cm}^{-2}$  [5]. With proper engineering of the MOS-structure, such as fluorinated gate dielectrics [22]–[24], plasma-based interface treatment [20], and thermal treatment [20], [25],  $n_{it}$  is expected to be greatly reduced. Therefore, there is a large room for boosting up  $V_{th}$ .

#### IV. CONCLUSION

A comprehensive analytical investigation of the charge distribution and gate control of the normally-off GaN DC-MOS-HEMT is presented in this paper. The correctness of the modeling has been verified by numerical simulations. A valuable insight into the principles of the DC-MOS-HEMT is gained based on the analytical modeling. The location of the AlN-ISL is found to be a critical parameter to determine the 2DEG distribution among the two channels, but it does not appreciably impact the total 2DEG density. At the gated region, the gate turns on the lower and upper channel sequentially. The sensitivity of  $V_{th}$  against the gate recess depth is dependent on the electric field in the upper channel layer originating from the space charges in the buffer ( $n_{buf}$ ). As  $n_{buf}$  is typically low, the DC-MOS-HEMT exhibits a robustness in  $V_{th}$  control. The analytical models developed in this paper provide a guidance for the design of the DC-MOS-HEMT.

#### REFERENCES

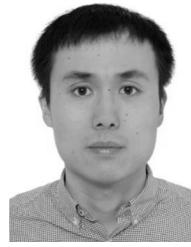
- [1] W. Huang, Z. Li, T. P. Chow, Y. Niiyama, T. Nomura, and S. Yoshida, "Enhancement-mode GaN hybrid MOS-HEMTs with  $R_{on,sp}$  of  $20 \text{ m}\Omega\text{-cm}^2$ ," in *Proc. ISPSD*, Orlando, FL, USA, May 2008, pp. 295–298, doi: [10.1109/ISPSD.2008.4538957](#).
- [2] B. Lu, M. Sun, and T. Palacios, "An etch-stop barrier structure for GaN high-electron-mobility transistors," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 369–371, Mar. 2013, doi: [10.1109/LED.2012.2237374](#).
- [3] S. Liu *et al.*, " $\text{Al}_2\text{O}_3/\text{AlN}/\text{GaN}$  MOS-channel-HEMTs with an AlN interfacial layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 723–725, Jul. 2014, doi: [10.1109/LED.2014.2322379](#).
- [4] B. Lu, O. I. Saadat, and T. Palacios, "High-performance integrated dual-gate AlGaIn/GaN enhancement-mode transistor," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 990–992, Sep. 2010, doi: [10.1109/LED.2010.2055825](#).
- [5] J. Wei *et al.*, "Low on-resistance normally-off GaN double-channel metal-oxide-semiconductor high-electron-mobility transistor," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015, doi: [10.1109/LED.2015.2489228](#).
- [6] J. Wei *et al.*, "Enhancement-mode GaN double-channel MOS-HEMT with low on-resistance and robust gate recess," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 225–228, doi: [10.1109/IEDM.2015.7409662](#).
- [7] K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto, and H. Shimawaki, "A normally-off GaN FET with high threshold voltage uniformity using a novel piezo neutralization technique," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Dec. 2009, pp. 153–156, doi: [10.1109/IEDM.2009.5424398](#).
- [8] J. Wei, J. Lei, X. Tang, B. Li, S. Liu, and K. J. Chen, "Channel-to-channel coupling in normally-off GaN double-channel MOS-HEMT," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 59–62, Jan. 2018, doi: [10.1109/LED.2017.2771354](#).
- [9] J. Lei *et al.*, "650-V double-channel lateral Schottky barrier diode with dual-recess gated anode," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 260–263, Feb. 2018, doi: [10.1109/LED.2017.2783908](#).
- [10] J. Lei *et al.*, "An interdigitated GaN MIS-HEMT/SBD normally-off power switching device with low ON-resistance and low reverse conduction loss," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2017, pp. 609–612, doi: [10.1109/IEDM.2017.8268456](#).
- [11] N. Goyal and T. A. Fjeldly, "Analytical modeling of AlGaIn/AlN/GaN heterostructures including effects of distributed surface donor states," *Appl. Phys. Lett.*, vol. 105, no. 2, p. 023508, 2014, doi: [10.1063/1.4890469](#).
- [12] Z. Wang, B. Zhang, W. Chen, and Z. Li, "A closed-form charge control model for the threshold voltage of depletion- and enhancement-mode AlGaIn/GaN devices," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1607–1612, May 2013, doi: [10.1109/TED.2013.2252466](#).
- [13] C. Wood and D. Jena, *Polarization Effects in Semiconductors: From Ab Initio Theory to Device Applications*. New York, NY, USA: Springer, 2008.
- [14] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaIn/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, doi: [10.1063/1.369664](#).
- [15] J. Würfl *et al.*, "Techniques towards GaN power transistors with improved high voltage dynamic switching properties," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2013, pp. 144–147, doi: [10.1109/IEDM.2013.6724571](#).
- [16] B. Bakeroot, A. Stockman, N. Posthuma, S. Stoffels, and S. Decoutere, "Analytical model for the threshold voltage of p-(Al)GaIn high-electron-mobility transistors," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 79–86, Jan. 2018, doi: [10.1109/TED.2017.2773269](#).
- [17] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, "Vertical leakage/breakdown mechanisms in AlGaIn/GaN-on-Si devices," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1132–1134, Aug. 2012, doi: [10.1109/LED.2012.2200874](#).
- [18] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaIn/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 77, no. 2, pp. 250–252, 2000, doi: [10.1063/1.126940](#).
- [19] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, and D. Jena, "Presence and origin of interface charges at atomic-layer deposited  $\text{Al}_2\text{O}_3/\text{III-nitride}$  heterojunctions," *Appl. Phys. Lett.*, vol. 99, no. 19, p. 193504, Nov. 2011, doi: [10.1063/1.3658450](#).
- [20] T.-H. Hung, P. S. Park, S. Krishnamoorthy, D. N. Nath, and S. Rajan, "Interface charge engineering for enhancement-mode GaN MISHEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 312–314, Mar. 2014, doi: [10.1109/LED.2013.2296659](#).
- [21] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007.
- [22] C. Chen *et al.*, "Fabrication of enhancement-mode AlGaIn/GaN MISHEMTs by using fluorinated  $\text{Al}_2\text{O}_3$  as gate dielectrics," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1373–1375, Oct. 2011, doi: [10.1109/LED.2011.2162933](#).
- [23] Y.-H. Wang *et al.*, "6.5 V high threshold voltage AlGaIn/GaN power metal-insulator-semiconductor high electron mobility transistor using multilayer fluorinated gate stack," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 381–383, Apr. 2015, doi: [10.1109/LED.2015.2401736](#).
- [24] Y. Zhang, M. Sun, S. J. Joglekar, T. Fujishima, and T. Palacios, "Threshold voltage control by gate oxide thickness in fluorinated GaN metal-oxide-semiconductor high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 103, no. 3, p. 033524, 2013, doi: [10.1063/1.4815923](#).
- [25] Q. Zhou *et al.*, "7.6 V threshold voltage high-performance normally-off  $\text{Al}_2\text{O}_3/\text{GaN}$  MOSFET achieved by interface charge engineering," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 165–168, Feb. 2016, doi: [10.1109/LED.2015.2511026](#).



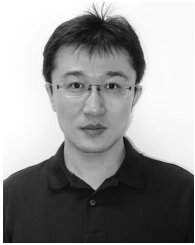
**Jin Wei** (S'15–M'18) received the B.S. degree from Sun Yat-sen University, Guangzhou, China, the M.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, and the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong.



**Meng Zhang** received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China. She is currently pursuing the Ph.D. degree with the Department of Industrial and Systems Engineering, The Hong Kong Polytechnic University, Hong Kong.



**Xi Tang** (S'14) received the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2017.



**Baikui Li** (M'14) received the B.S. and B.B.A. degrees from the University of Science and Technology of China, Hefei, China, and the Ph.D. degree from the Department of Physics, The Hong Kong University of Science and Technology, Hong Kong.

He is currently an Associate Professor with the College of Optoelectronic Engineering, Shenzhen University, Shenzhen, China.



**Kevin J. Chen** (M'96–SM'06–F'14) received the B.S. degree from Peking University, Beijing, China, and the Ph.D. degree from the University of Maryland, College Park, MD, USA.

He is currently a Professor with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong.

Dr. Chen is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.