A ± 3 ppm/°C Single-Trim Switched Capacitor Bandgap Reference for Battery Monitoring Applications

Bradford L. Hunter, *Member, IEEE*, and Wallace E. Matthews, *Member, IEEE*

***Abstract*— A precision bandgap reference has been developed in a 0.18 μm BiCMOS process that achieves ±3 ppm/°C temperature drift at ±3 σ from -40 °C to 110 °C. The reference is designed to utilize single temperature trim and standard components. A 3.65 V switched capacitor reference voltage is provided to a 2nd order delta-sigma modulator ADC to digitize a battery cell voltage. The switched capacitor reference utilizes fully differential sampling which reduces the errors from channel charge injection and clock feedthrough introduced by pseudo-differential sampling. A new technique for sampling a V_{be} voltage directly onto the output of the reference's differential amplifier has been developed that removes the error that would be introduced from differentially sampling the V_{be} and the ΔV_{be} voltage terms independently. The bandgap reference and ADC combination have an input referred noise spectral density of 4.7 $\mu V/\sqrt{Hz}$ from 0.1 to 162 Hz yielding 15 stable output bits.**

***Index Terms*— Bandgap reference, delta-sigma conversion, battery monitor, room temperature trim, switched capacitor.**

I. Introduction

THERE has been a proliferation of the use of portable electronic devices in the past several decades. Portable electronics almost exclusively require batteries to operate and an accurate indication of the state of charge of the battery improves the user experience. Lithium ion (Li-Ion) batteries are popular in portable battery applications due to the high cell energy density [1]. Li-Ion cells have a typical usable voltage range from 3.0 V to 4.0 V, which varies depending upon the exact cell chemistry. The cell voltage exhibits a relatively small change in level as a function of the percentage of the state of charge. For example, the voltage change can be 300 mV from 90% to 10% state of charge [1]. Many battery monitoring systems aim to achieve ±1% accuracy on state of charge which can translate for gauging algorithms to ±1% voltage accuracy out of 300 mV, or ±0.075% out of 4.0 V. Achieving the target accuracy over a temperature range from -40 °C to 110 °C requires a reference voltage with less than ±5 ppm/°C temperature drift. As a result there is a demand for precision bandgap references in integrated circuits used for portable battery applications to provide the best indication of the state of charge of the battery.

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The authors are with Texas Instruments, Austin, TX 78733 USA (e-mail: blhunter@ti.com; ed.matthews@ti.com).

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The largest source of error in most band gap references is the error amplifier offset voltage [2]. Various implementations of continuous time CMOS and BiCMOS bandgap references have been presented with a range of techniques for removing the error amplifier offset, including offset trimming and amplifier chopping [3]–[6]. In battery cell voltage measurement applications, the bandgap reference is utilized by an ADC. The ADC is required because the system must provide cell state of charge information in a digital format. In a discrete time switched capacitor based ADC the reference voltage does not need to be continuous time. Therefore, a switched capacitor based implementation of the reference is viable [2]. Switched capacitor bandgap references have the benefit of being able to easily remove the error amplifier offset with auto-zeroing as a part of the natural switching process to generate an output reference voltage. A pseudo-differential switched capacitor bandgap reference can have the disadvantage of introducing an error term from channel charge injection and clock feedthrough on the charge conservation nodes of the switched capacitor amplifier.

This paper introduces a fully differential switched capacitor bandgap reference with a new technique for developing the differential reference. Section IV provides the description of an error term that is introduced from differentially sampling the V_{be} and the ΔV_{be} voltage terms independently in a traditional manner. To remove this error term, the V_{be} voltage is sampled onto the output of the reference's differential amplifier centered with respect to a common mode voltage. This technique offers superior drift performance for a single temperature trim reference.

The resulting fully differential reference achieves ±3 ppm/°C voltage drift from -40 °C to 110 °C. The reference was implemented using standard components in a 0.18 μm BiCMOS process technology, using 0.8 μm 5 V devices. The ADC output code is gain and temperature drift corrected digitally, similar to that described in [6], [7] and [12], [13], to avoid the need for analog second order curvature correction. The resulting drift performance is shown to be nearly two times better than prior work [3]–[11] with a single temperature trim.

The paper is organized into five major sections. Section II presents the system architecture of the test chip. Section III outlines the underlying mechanics and techniques for achieving precision accuracy in a single temperature trim bandgap reference. Section IV describes the circuit design techniques used to implement the precision bandgap reference. Section V presents the hardware results of the physical implementation and Section VI provides conclusions.

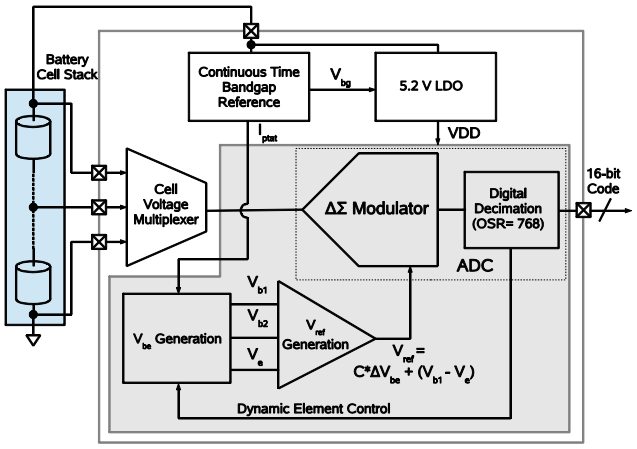

Fig. 1. Battery monitor and precision bandgap reference system diagram.

II. System Architecture

Fig. 1 depicts the system diagram of the precision bandgap reference test chip. A battery cell stack provides power to a continuous time bandgap reference and an integrated 5.2 V LDO. The continuous time bandgap reference supports a precision reference by providing a PTAT bias current (I_{ptat}). The continuous time bandgap also provides a reference to the LDO that generates VDD. The integrated LDO powers the precision bandgap reference and the ADC. The precision reference is composed of a V_{be} generation circuit that provides diode bias voltages to a V_{ref} generation circuit.

As a measured battery cell voltage can reach up to 4.5 V, a 3.65 V reference voltage was selected to minimize the impact of power supply and thermal noise relative to the reference voltage. The battery cell voltage is divided by 1.7 at the input to the ADC using a switched capacitor scale factor. The system operates at a minimum input voltage of 6 V which makes the design suitable for applications using 3 or more series Li-Ion cells. For applications requiring 1 or 2 cell support, the reference voltage could be reduced to 1.2 V or 2.4 V accordingly. The analog circuits were implemented with 5 V tolerant transistors with a minimum available channel length for switches of 0.8 μm.

The ADC is implemented with a 2nd order delta-sigma modulator with discrete time switched capacitor integrators in a cascade feedback form. The digital decimation filter is a sinc^3 cascade with N equal to 256 [14]. As the precision bandgap reference voltage is not continuous time, the reference voltage must be inferred through the ADC 16-bit output code provided by the decimation filter. The input clock frequency is 500 kHz and is divided by 2 to provide an ADC sample rate of 250 kHz and a conversion rate of approximately 325 S/s at an OSR of 768.

III. Single Temperature Trim Analysis

The target accuracy for the design was ±2 mV measuring a 3V battery cell voltage from -40 °C to 110 °C after a digital gain and temperature drift correction. The resulting reference temperature drift can be no greater than ±4.4 ppm/°C over the same temperature range with respect to 3.65 V.

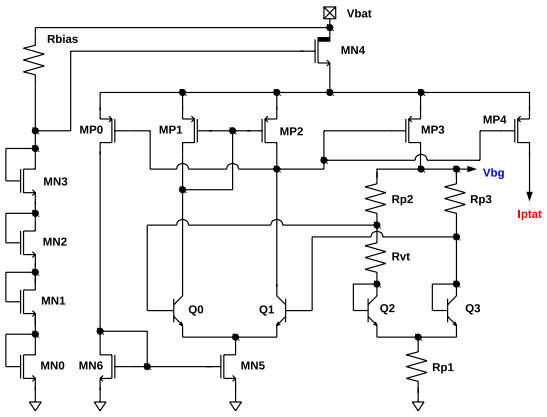

Fig. 2. Continuous time bandgap reference circuit schematic.

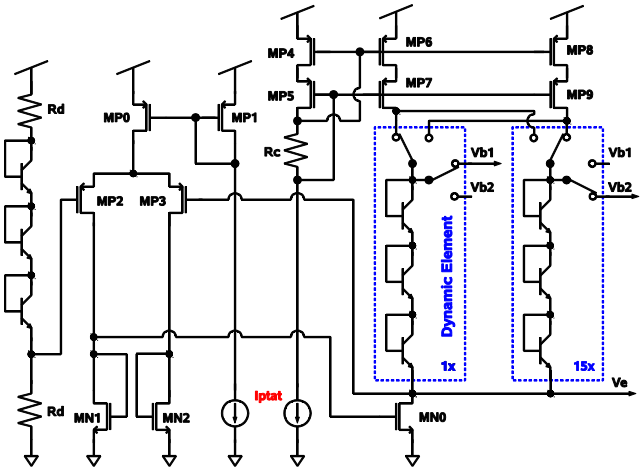

Fig. 3. V_{be} generator circuit schematic.

Fig. 2 shows the circuit schematic for the continuous time bandgap reference. The bandgap reference is powered from the external battery voltage (V_{bat}) that is pre-regulated with a high voltage tolerant drain extended source follower nFET device MN4. The bandgap reference provides I_{ptat} for the V_{be} generator and a bandgap voltage output (V_{bg}) for the LDO. The start-up circuit is not shown for simplicity and device MP0 provides a means for self-biasing the error amplifier. The typical current consumption of the continuous time bandgap reference is 4 μA and the physical area is 0.064 mm^2. The PTAT bias current magnitude as a function of temperature can be written as

$$I_{ptat} = \frac{V_t \ln(x)\, M}{R_{vt}} \tag{1}$$

R_{vt} is the resistor that drops the voltage difference between the bipolar devices Q2 and Q3, with a size ratio of x. M is any adjustment in the current magnitude from device ratios through current mirroring. V_t is the thermal voltage. For this design, R_{vt} equals 100k Ohms, x equals 8, and M equals 4, yielding an I_{ptat} at 25 °C of 2 μA shown in Fig. 3. When mirrored, I_{ptat} should be cascoded to avoid sensitivity to VDD variations. The bipolar devices selected throughout this design were vertical NPN with a typical β_f of 120 and an emitter area of 76 μm^2 per device.

I_{ptat} can also be rewritten as shown in [15].

$$I_{ptat} = GT^{\alpha} \tag{2}$$

G is a temperature independent constant and α models the temperature dependence of I_{ptat}. Fig. 3 shows the circuit schematic for the V_{be} generator. The PTAT current is mirrored at equal values into a pair of bipolar transistors acting as diode strings to generate a pair of diode voltages in the V_{be} generator. Ignoring the effects of finite β_f and non-zero base resistance, the V_{be} voltage can be written as.

$$V_{be} = V_{b1} - V_e = 3V_t \ln\left(\frac{I_{ptat}}{I_s} M\right)$$
$$\Delta V_{be} = V_{b1} - V_{b2} = 3V_t \ln(x) \tag{3}$$

I_s is the saturation current of the bipolar device, x is the bipolar device emitter size ratio, set to 15, M is the W/L ratio of MP6 and MP8 to MP4, set to 16, and V_e is defined by a bias generator to be approximately equal to.

$$V_e = \frac{Vdd}{2} - 1.5V_t \ln\left(\frac{Vdd - 2}{R_d I_s}\right) \tag{4}$$

The selected value of R_d was 50k Ohms.

Dynamic element matching is introduced in the V_{be} generation circuit to reduce error terms associated with V_{be} voltage mismatch by a factor equal to the diode ratio, in this case 15 [12]. The dynamic elements are switched every 6 cycles such that each of the 16 diode strings contributes to the single sampled diode voltage 8 times over the course of a conversion at the selected 768 OSR.

The current sources composed of devices MP6 and MP8 were not dynamically matched. The gate area of each device was set to 34 000 μm^2 to minimize V_{th} mismatch. The over drive (V_{ov}) of the devices was in excess of 300 mV to minimize g_m and minimize drain current mismatch as described in [16].

The final reference voltage generated with a switched capacitor ratio C multiplied by the PTAT ΔV_{be} voltage (3) can be written as

$$V_{ref} = C\Delta V_{be} + V_{be} \tag{5}$$

For temperature stability of a precision reference, the change in V_{ref} with respect to temperature is of particular importance. The derivative of V_{ref} with respect to temperature is given in [15] to be approximately

$$\frac{dV_{ref}}{dT} = (4 - n - \alpha)\frac{V_t}{T}\left(\frac{T_0 - T}{T}\right) \tag{6}$$

n is the exponent of the mobility variation in the base of the bipolar transistor (typically about 0.8) and T_0 is the temperature where dV_{ref}/dT equals to 0. The application calls for T_0 to be 25 °C. The V_{ref} voltage at T_0 is henceforth referred to as the Minimum Temperature Coefficient (MTC) voltage. Fig. 4 shows the benefit of biasing the V_{be} generator diode string with a PTAT current. Increasing dI_{ptat}/dT effectively increases α in (2) thereby reducing the magnitude of the derivative of V_{ref} versus temperature in (6). The associated change in G from (2) also adjusts the MTC voltage.

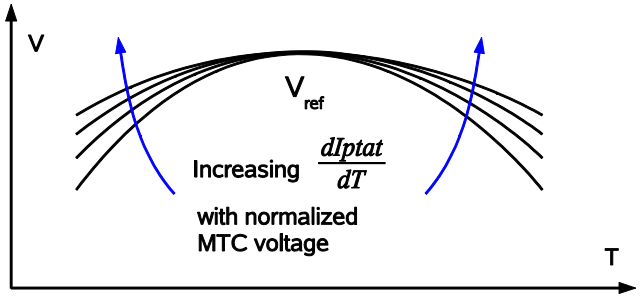

Fig. 4. V_{ref} voltage as a function of temperature and I_{ptat}.

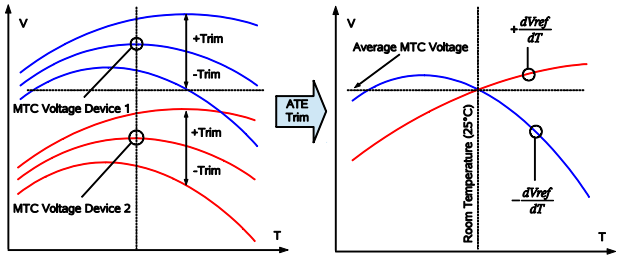

Fig. 5. Two devices with different MTC voltages trimmed with an ATE to the average MTC voltage.

A single temperature ATE trim scheme requires that the MTC voltage be the same for all devices to achieve precision. Second order digital error correction of temperature drift also requires that dV_{ref}/dT be similar for all devices. Fig. 5 illustrates the impact of two devices having different MTC voltages and the associated difference in dV_{ref}/dT after a single temperature ATE trim.

After applying dynamic element matching, the remaining significant error sources that contribute to the adjustments in the MTC voltage are non-PTAT terms that include global β_f variation, global base resistance variation, and I_{ptat} current variation via the terms G and α in (2). β_f variation and base resistance variation can be reduced by selecting a bipolar transistor with the highest possible current gain. If β_f is sufficiently low, [17] presents alternative techniques for current biasing the bipolar devices to reduce the temperature drift error from β_f variations. I_{ptat} variation can be somewhat addressed by measuring the I_{ptat} current magnitude on the ATE and performing a room temperature trim prior to performing the MTC voltage trim, although this technique was not implemented on the test chip. I_{ptat} trim is estimated to improve drift performance by up to 20%.

IV. Circuit Design

A. Design for DC Precision

This work aims to largely eliminate the error sources introduced from generating the discrete time reference with switched capacitor circuits. Fig. 6 shows a pseudo-differential switched capacitor circuit that generates V_{ref} while auto-zeroing the error amplifier. Here pseudo-differential sampling is defined by a differential input voltage sampled by a single ended amplifier. When switch MN0 opens, transitioning from φ_1 to φ_2, an undesired error term is introduced from channel

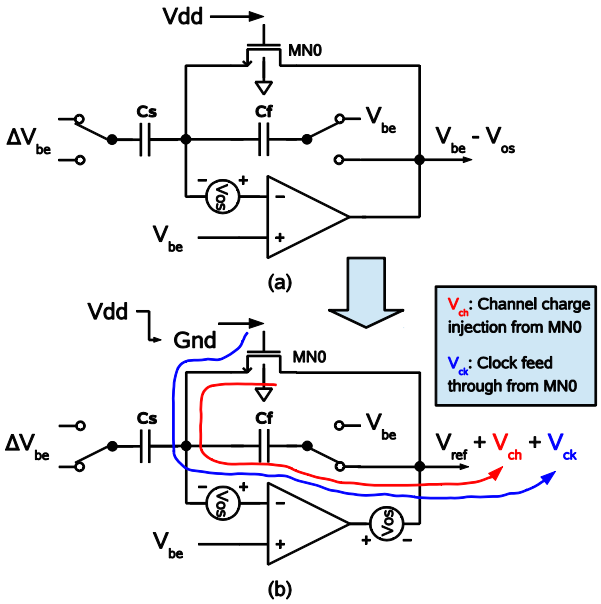

Fig. 6. Pseudo-differential switch capacitor circuit for generating V_{ref}: (a) φ_1 (b) φ_2.

charge injection and clock feedthrough described in [18] and rewritten below.

$$V_{ch} = WLC_{ox}\left(\frac{Vdd - V_{be1} - V_{th}}{2\left(C_s + C_p\right)}\right)$$
$$V_{ck} = Vdd\left(\frac{WC_{ov}}{WC_{ov} + C_s + C_p}\right) \quad (7)$$

C_{ox} is the oxide capacitance, C_{ov} is the polysilicon to source overlap capacitance, W and L are the channel width and length, and V_{th} is the threshold voltage of device MN0. C_p is the parasitic capacitance seen on the net connected to the input of the error amplifier. The error terms V_{ch} and V_{ck} appear at the output of the error amplifier in φ_2 and are not canceled by auto-zeroing. Both error sources have a dependence upon VDD which will adjust the MTC voltage as a function of VDD. The channel charge injection error has a dependence upon V_{th} which introduces an error term that adjusts the MTC voltage and temperature drift as well. Dummy device cancellation techniques only somewhat eliminate these error sources [18]. A fully differential switched capacitor topology limits these error sources more effectively to within the matching of the differential switch pair. A fully differential implementation has the additional benefit of reduced sensitivity to power and ground supply noise compared to pseudo-differential and single ended counterparts.

Fig. 7 shows the switched capacitor circuit that generates the differential reference voltage (5). The common mode voltage (V_{cm}) was set to VDD/2. Fig. 8 shows the non-overlapping clock control scheme for the switched capacitor amplifier. φ_1, φ_{1D}, φ_2 and φ_{2D} are utilized by the reference generator while φ_3, φ_{3D}, φ_4 and φ_{4D} are utilized by the ADC. The reference generator circuit must operate with φ_1 and φ_2 at twice the frequency of the ADC in order to introduce an extra phase for auto-zeroing.

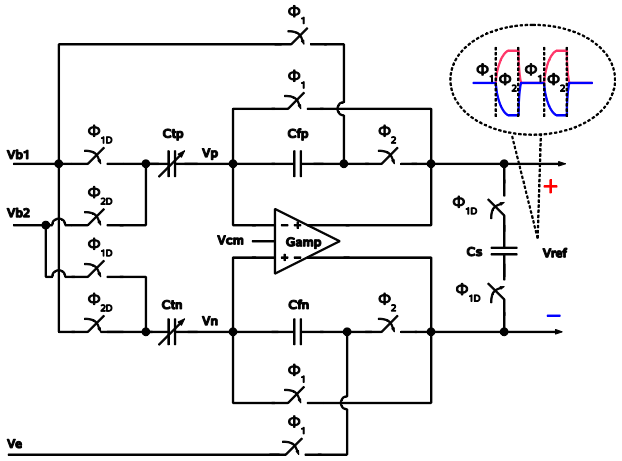

Fig. 7. V_{ref} generator circuit schematic.

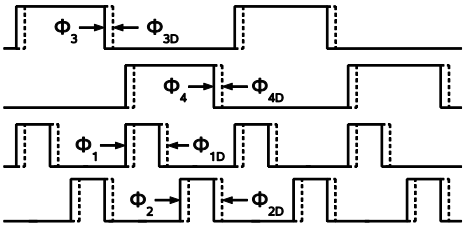

Fig. 8. V_{ref} generator and ADC Clock phase timing diagram.

With a differential implementation comes the problem of introducing two independent voltage gain terms to generate V_{ref} differentially at the output of differential amplifier (G_{amp}) around V_{cm}. For the pseudo-differential switched capacitor reference shown in Fig. 6, V_{be} is stored on the back plate of the feedback capacitor (C_f) in the auto-zeroing phase. The output reference voltage is then the V_{be} voltage plus the addition of the ΔV_{be} term times the ratio of C_s/C_f. If the V_{be} voltage cannot be forced directly onto the output of the switched capacitor amplifier, the following alternative derivation of V_{ref} can be generated fully differentially.

$$V_{ref} = \frac{C_{s1}}{C_f}\Delta V_{be} + \frac{C_{s2}}{C_f}V_{be1} \quad (8)$$

C_{s1} and C_{s2} are separate input sample capacitors that can provide separate weighting for each term. However, the ability to accurately trim V_{ref} to the MTC voltage at a single temperature with mismatch between C_{s1} and C_{s2} is not possible. Dynamic element matching C_{s1} and C_{s2} only partially eliminates the matching error and introduces added control complexity, especially when considering the need for a fine trim. The generation of V_e using the error amplifier and dummy bias leg in the V_{be} generator can remove the error source entirely. V_{b1} and V_e are differentially sampled on the output of G_{amp} centered around V_{cm} so that the need for C_{s2} in (8) is eliminated. The modified derivation of V_{ref} generated from the circuit shown in Fig. 7 is given by

$$V_{ref} = 2 * \left(\frac{C_{tp} + C_{tn}}{C_{fp} + C_{fn}}\right)\Delta V_{be} + V_{be} \quad (9)$$

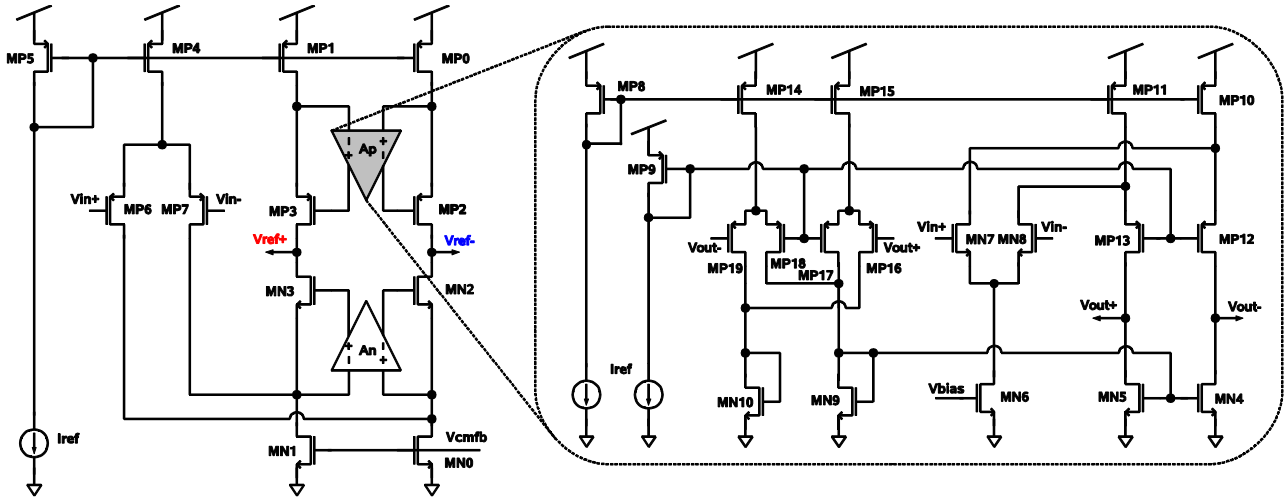

Fig. 9. High gain amplifier (G_{amp}) and gain boosting amplifier (Ap) circuit schematic.

Splitting half of the units of C_{s1} and C_f differentially into two equal parts to create C_{tp}, C_{tn}, C_{fp}, and C_{fn} does not introduce any additional error sources beyond the pseudo-differential counterpart after an ATE trim. Mismatch between the split pairs of capacitors generates a small change in the common mode voltage that is rejected by the differential ADC sampling process.

The switched capacitors in Fig. 7 were implemented with standard 3-level metal to metal capacitors with a density of 0.4 fF/μm^2. The feedback capacitor values, C_{fp} and C_{fn}, were 340 fF and the sampling trim capacitors, C_{tp} and C_{tn}, were 1.36 pF. Of the 1.36 pF composing C_{tp} and C_{tn}, ±50 fF were trimmed with 7 bits providing an LSB trim capacitor size of approximately 0.8 fF. This provided a trim step of approximately 1 mV on the 3.65 V reference, adjusting the MTC voltage to within ± 500 μV of the intended value using the ATE.

Fig. 9 shows the circuit schematic of G_{amp} and the pFET cascode gain boosting amplifier (A_p). The common mode feedback control signal V_{cmfb} was generated with a standard switched capacitor circuit described in [15]. A single stage folded cascode topology was selected to utilize the output load capacitance to form the dominant pole. Gain boosting was introduced to increase the amplifier gain to approximately 125 dB with the output voltages at the common mode in φ_1. When the output voltages of G_{amp} were increased to ±1.8V around V_{cm}, the gain was reduced to 95 dB in φ_2 which yielded a gain error on the reference voltage below 100 μV. The high gain also ensured robust cancellation of the input offset voltage of G_{amp}, estimated to be ±3 mV at ± 3 σ.

The nFET cascode gain boosting amplifier (A_n) was a complement of the topology of A_p. A continuous time common mode voltage control scheme was selected for the gain boosting amplifiers as the output voltages were not subject to large voltage swings. The common mode voltage was set by the V_{gs} of device MP9. The selected common mode biasing scheme provides reliable control of the gain boosting amplifier output voltages across a wide PVT range.

Fig. 10 shows the interface between the reference voltage and the first integrator of the ADC. The ADC integrator

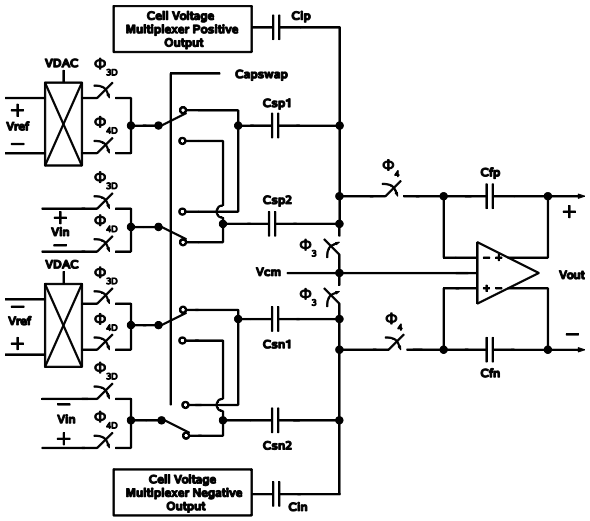

Fig. 10. V_{ref} generator to ADC interface circuit schematic.

amplifier includes amplifier chopping, not shown, similar to that described in [17]. VDAC controls the polarity of the reference voltage into the ADC based on the output of the delta sigma modulator quantizer. An additional control signal entitled Capswap is introduced to the inputs of the ADC sampling capacitors C_{sp1} and C_{sp2}. Two trims on the ATE with Capswap set high and low reduces the mismatch error introduced by C_{sp1} and C_{sp2}. C_{sp1}, C_{sp2}, C_{sn1} and C_{sn2} were selected to be 250 fF. C_{ip} and C_{in} were selected to be 150 fF to introduce a scaling factor on the cell input voltage.

B. Design for Transient Precision

For reference voltages being sampled by a discrete time ADC, sufficient voltage settling is critical to achieving precision. A target settling voltage of within 100 μV of the final value of the reference was selected. At 500 kHz, the available settling time per phase for the V_{be} and V_{ref} generator circuits is 1 μs. With an exponential settling behavior the number of required time constants to achieve the target settled voltage is 10. Assuming G_{amp} settles to within a single time constant

at the inverse of the gain bandwidth, then the required gain bandwidth is at least 10 MHz. The required gain bandwidth will be denoted as f_s. In practice the settling performance will exceed 100 μV because the amplifier transitions through a non-linear slewing region for a time T_s at the start of each phase. Higher order poles will improve the settling time as well [19].

Considering the settling of G_{amp}, the circuit operates in two distinct phases with two different closed loop gain factors. In φ_1 the amplifier input is shorted to the output and the unity gain bandwidth is given by the following expression.

$$Gbw = \frac{g_{m_{MP6}} + g_{m_{MP7}}}{4\pi C_{l_{\varphi 1}}} \tag{10}$$

$C_{l\varphi 1}$ is the output load capacitance driven by G_{amp} which is composed of the ADC input capacitance (approximately 1 pF total), the sample capacitance (C_{tp} and C_{tn}), and the parasitic capacitance at net V_p and V_n (C_{pp} and C_{pn} of approximately 1 pF total). C_{pp} and C_{nn} are composed mostly of the input capacitance of G_{amp}. In φ_2 the unity gain bandwidth is reduced by approximately the following factor.

$$\begin{aligned} C_{l_{\varphi 1}} &= C_{pp} + C_{tp} + C_l \\ C_{l_{\varphi 2}} &= \left(C_{pp} + C_{tp}\right) \frac{\left(C_{pp} + C_{tp} + C_{fp}\right)}{C_{fp}} + C_l \\ R &= \frac{C_{l_{\varphi 2}}}{C_{l_{\varphi 1}}} \end{aligned} \tag{11}$$

$C_{l\varphi 1}$ and $C_{l\varphi 2}$ are the effective output load capacitances seen by G_{amp} in φ_1 and φ_2 respectively. Using the capacitor values provided earlier, $C_{l\varphi 1}$ was calculated to be 3.4 pF, $C_{l\varphi 2}$ was calculated to be 19.7 pF, and the gain bandwidth reduction factor was calculated to be 5.8. The gain bandwidth reduction creates a gain bandwidth mismatch between the two phases. If the required 10 MHz unity gain bandwidth is set in φ_2, then the gain bandwidth in φ_1 would be 5.8 times higher due to the change in the amplifier load capacitance. The excess bandwidth can be problematic from a stability stand point because at 58 MHz in φ_1 other non-dominant poles begin to degrade the stability performance of G_{amp}. In particular, the pole introduced from the switches in parallel with C_{fp} and C_{fn} and in series with C_{tp} and C_{tn} will require the W/L ratio of the switch to be large. To avoid the introduction of charge injection and clock feedthrough error from switch mismatches, the switch W/L ratio should be the minimum allowable by the technology at the minimum available L (0.8 μm). Therefore, limiting the bandwidth of G_{amp} to 10 MHz in both phases is beneficial to achieving optimal performance. With the introduction of C_s, shown in Fig. 7, activated only in φ_1 as a gain bandwidth matching capacitance, the excess bandwidth in φ_1 is reduced. The gain bandwidth in φ_2 is left unchanged. An expression for the value of C_s that yields matching bandwidth can be written as follows.

$$C_s = \frac{C_{l_{\varphi 2}} - C_{l_{\varphi 1}}}{2} \tag{12}$$

The reduction factor of 2 comes from the fully differential connection of capacitor C_s. In this design, C_s was set to 8 pF to reduce the φ_1 unity gain bandwidth to approximately 10 MHz. Fig. 11 illustrates the bandwidth matching technique with a Bode plot.

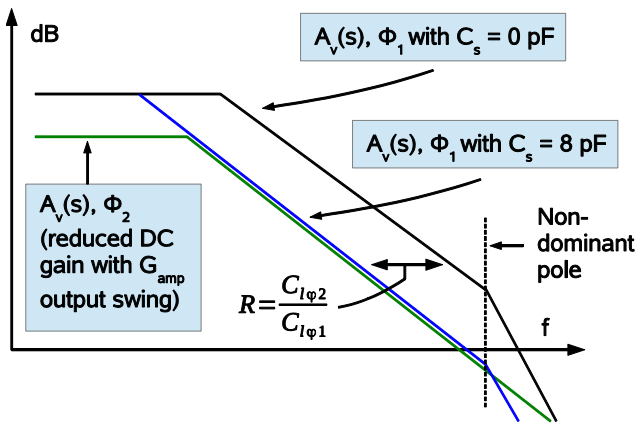

Fig. 11. Bode plot of the open loop gain of G_{amp} in φ_1 and φ_2, illustrating the bandwidth matching technique.

To calculate the required bias current of MP4 in Fig. 9, assuming moderate inversion for MP6 and MP7, we use the following equation.

$$I_{d_{MP4}} = 2\pi f_s C_{l_{\varphi 2}} n V_t 2 \tag{13}$$

n is the fitting factor for moderate inversion of 2.5. With $C_{l\varphi 2}$ of 19.7 pF, the required bias current was estimated to be 155 μA. In the final design, a bias current of 192 μA was selected for MP4 and 96 μA for MP1 and MP0 in the V_{ref} generator.

The gain boosting amplifier gain bandwidths were both set to be approximately 2 times higher than the gain bandwidth of G_{amp}. A description of the analysis of the optimization of the gain bandwidth of the gain boosting amplifiers can be found in [20].

The total current consumption of the V_{be} and V_{ref} generators combined was 750 μA, including the gain boost amplifiers and common mode bias generation. Combined with the ADC, the total current consumption of the system was approximately 1 mA during conversions. In battery management applications, the precision bandgap reference and ADC must only remain active while performing cell voltage measurements. In many modes of operation the precision bandgap reference can be active less than 1% of the time.

C. Simulation Results

Fig. 12 shows the simulation results of the finalized design. After applying a digital error correction to the voltage gain and temperature drift, the peak temperature drift of the reference was ±1.6 ppm/°C from -40 °C to 110 °C at ± 3 σ limits with respect to 3.7245 V. The reference voltage was measured in simulation at the input of the ADC. The simulation results were taken from Monte Carlo simulations. Corner simulations showed substantially better drift performance because the corner models did not include variation in the bipolar device parameters that affect the MTC voltage.

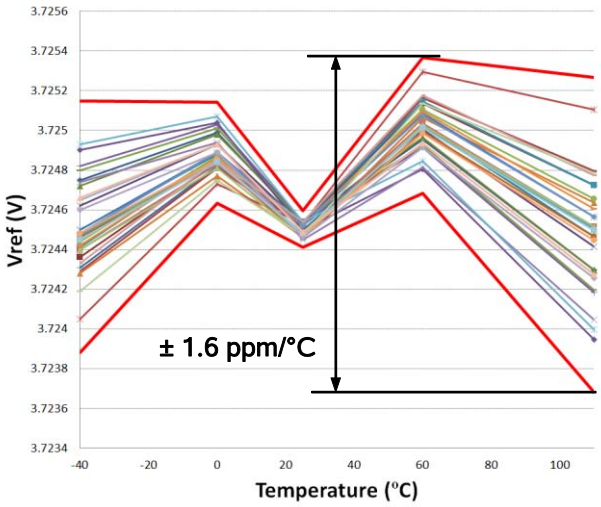

Fig. 12. Simulation results of V_{ref} temperature drift of 30 samples and ± 3 σ limits in bold red.

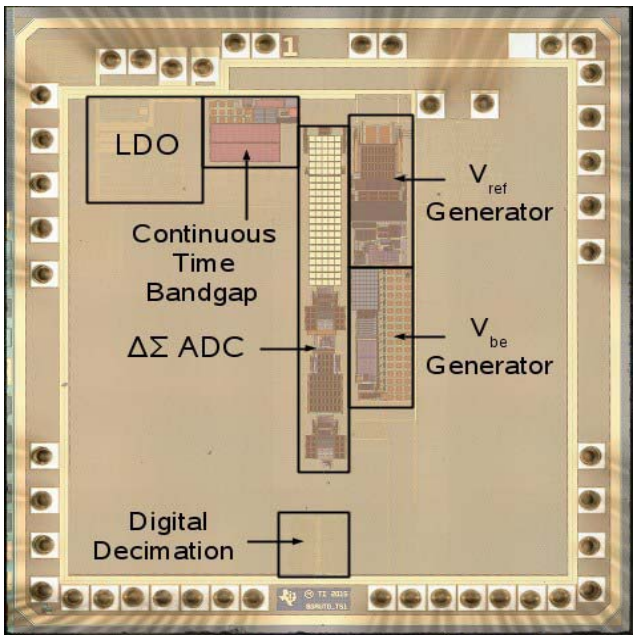

Fig. 13. Die micrograph, the die dimensions of the test chip were 1.9 mm^2 by 2.1 mm^2.

V. Hardware Results

Fig. 13 shows a die photo of the fabricated test chip. The automatic metal fill pattern generation was blocked over the accuracy critical circuits, but other circuits, such as the digital decimation filter and LDO, were covered by metal fill. The continuous time bandgap reference occupies 0.07 mm^2, the V_{be} and V_{ref} generators occupy 0.21 mm^2, and the ADC occupies 0.2 mm^2. 13 devices were placed in ceramic packages for temperature drift and noise characterization of the reference voltage.

Fig. 14 shows a plot of the bandgap reference voltage measured with Capswap set low and high. Fig. 15 shows the uncorrected temperature drift of the reference across the sample set. Based on the selected sample, the MTC voltage was found to be 3.657 V. Fig. 16 shows the temperature drift after voltage gain correction. Voltage gain correction is

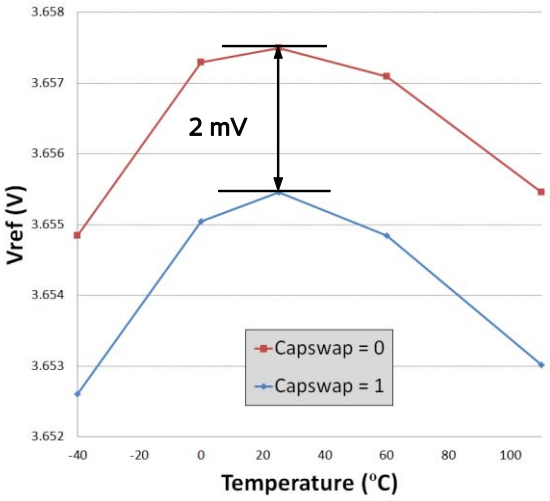

Fig. 14. V_{ref} temperature drift as a function of Capswap from hardware.

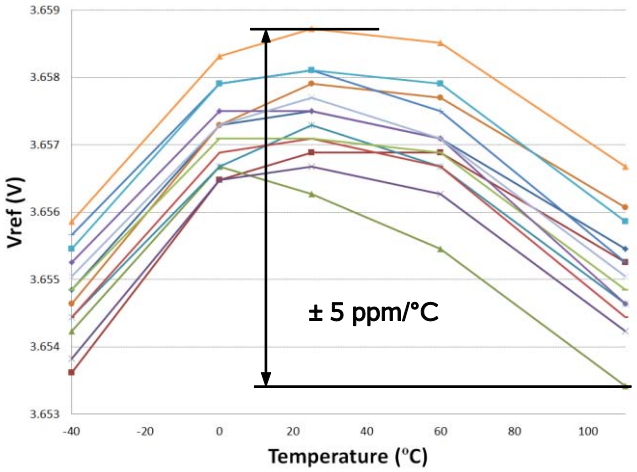

Fig. 15. Uncorrected V_{ref} temperature drift from 13 samples.

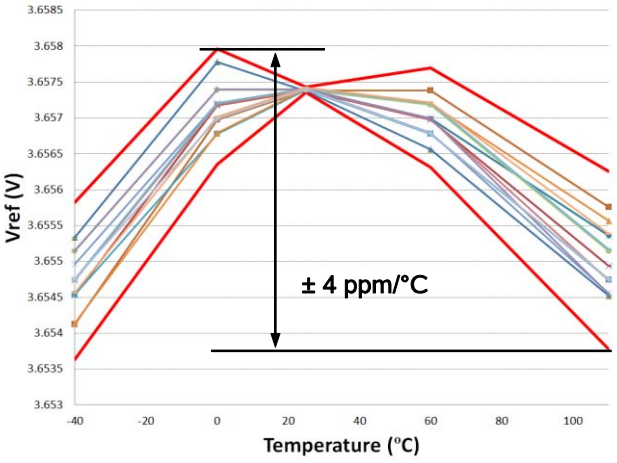

Fig. 16. Voltage gain corrected V_{ref} temperature drift from 13 samples with ± 3 σ limits in bold red.

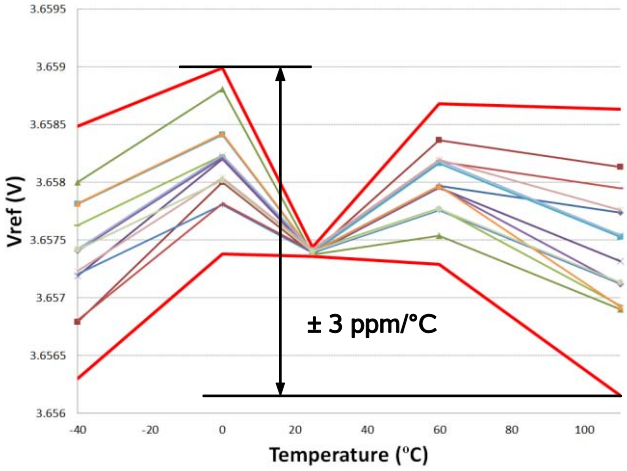

Fig. 17. Voltage gain and temperature drift digitally corrected V_{ref} temperature drift from 13 samples with $\pm$ 3 σ limits in bold red.

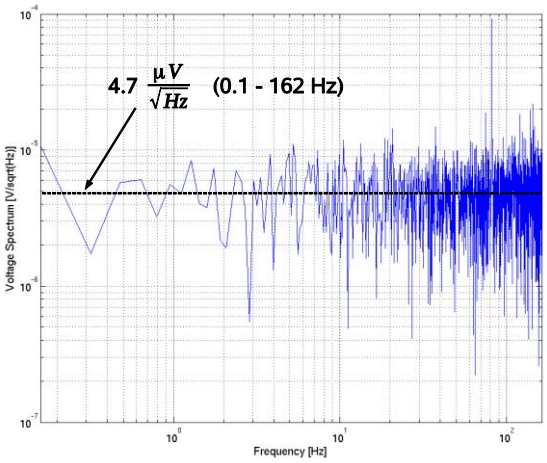

Fig. 18. Bandgap reference and ADC measured input referred voltage noise spectrum.

straightforward to implement digitally at the system level. The ADC output code that will yield the average MTC voltage at a fixed input voltage is known. Various gain error terms in the system, such as the selected Capswap setting, will adjust the ADC output code somewhat after the MTC voltage trim on the ATE is complete. The difference between the code read from the ADC after the MTC voltage trim and the expected output code can be stored as a gain adjustment factor. The gain adjustment factor can then be applied to the inferred reference voltage for ADC voltage measurement calculations by firmware at all temperatures to improve accuracy.

Fig. 17 shows the V_{ref} voltage after digital error correction for gain and temperature drift with the $\pm$ 3 σ limits highlighted in bold red. The corrected temperature at the 3 σ limits was $\pm$3 ppm/°C with respect to 3.6575 V. Performing digital temperature drift correction is more sophisticated at the system level and requires an integrated internal temperature sensor [7]. In battery management applications, an internal temperature sensor is multiplexed at the input to the ADC and measuring the internal die temperature with each battery cell measurement is a standard practice. Integrated firmware then applies a correction to the cell voltage measurement based on the measured temperature. For this work, the selected temperature compensation terms were set to 43 μV/°C for temperatures below 25 °C and 27 μV/°C for temperatures above 25 °C. For improved accuracy over a limited temperature range (such as 0 °C to 60 °C) a separate compensation term can be used for different temperature regions.

The error corrected temperature drift measured on the hardware was about 2 times greater than simulation. The reduction in drift performance can be partially explained by the wide variety of mismatch and temperature drift terms that are not captured in the simulation models (mismatches in parasitic capacitors and switch drain/source areas, etc.). There was also a reduction in the MTC voltage of about 2% in hardware that is commonly caused by minor modeling inaccuracies in the bipolar saturation current. In particular, a 2% error in the band gap voltage of silicon extrapolated to 0°K will generate a change to the intrinsic carrier concentration term of the saturation current that will cause a 2% adjustment to the MTC voltage [15].

The inferred reference voltage noise was measured by taking 2048 samples of the ADC output code with a 2 V input level. The resulting output code readings were converted back to voltages to reflect the noise to the input of the ADC and the spectrum was measured using an FFT. Fig. 18 shows the FFT of the quantized input voltage up to the conversion frequency divided by 2. The spectrum is mostly white with a total integrated noise of approximately 60 μV and a noise spectral density of 4.7 μV/$\sqrt{\text{Hz}}$ from 0.1 to 162 Hz. The following equation is used to calculate the code stability of the bandgap reference and ADC combination.

$$CS = log_2\left(\frac{2V_{ref}}{3.3\sigma_t}\right) \tag{14}$$

Where σ_t represents the single sigma total integrated noise reflected to the input of the ADC, which includes the bandgap reference noise, and the resulting CS was 15 bits.

The bandgap reference voltage was stable with respect to the battery voltage. The external input voltage was adjusted from 6 V to 32 V with a measured ADC output code change of 0.1 LSB yielding a PSRR of 127 dB with respect to the full scale range of 2 times V_{ref}. 32 V represents a typical stack voltage of 8 series Li-Ion battery cells.

Table I shows a comparison of this work with other previous works [3]–[11]. The current consumption is substantially higher in this work because the precision reference directly settles the voltage to the ADC for digitization. The effective current consumption of this work can be reduced by powering down the precision reference when not in use, as described at the end of Section IV B. This work achieves the minimum drift at a single temperature trim. [7] presents superior drift performance but requires 4 temperature trims adding significant test cost. A ppm metric normalizes the drift with respect to the magnitude of the reference voltage. Lower voltage references must be scaled more with respect to the battery voltage so the absolute voltage errors are increased by the scale factor, but the ppm drift remains unchanged. The active area includes the

TABLE I
PERFORMANCE COMPARISON

Parameter	This Work	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]
Year	2016	2011	2007	2005	2015	2015	2012	2015	2014	2015
Technology	0.8 µm BiCMOS	0.16 µm CMOS	0.35 µm CMOS	0.6 µm CMOS	0.13 µm CMOS	0.35 µm CMOS	0.5 µm BiCMOS	0.18 µm CMOS	0.18 µm CMOS	0.13 µm CMOS
Supply Voltage	5.2 V	1.8 V	1.4 V	1.8 V – 5.5 V	1.5 V	3.3 V	3.6 V	1.3 V- 2.6 V	1.2 V	1.2 V
Active Area	0.28 mm^2	0.12 mm^2	1.2 mm^2	1.2 mm^2	0.034 mm^2	0.44 mm^2	0.04 mm^2	0.05 mm^2	0.036 mm^2	0.063 mm^2
Bandgap Voltage	3.65 V	1.09 V	0.86 V	1.15 V	1.23 V	1.22 V	1.29 V	1.14 V	0.77 V	0.74 V
# of Samples	13	61	11	60	13	5	5	12	8	8
Temperature Range	-40°C to 110°C	-40C to 125°C	-20°C to 120°C	-40°C to 125°C	-40°C to 120°C	-40°C to 100°C	-40°C to 100°C	-55°C to 125°C	-40°C to 120°C	-40°C to 120°C
Current Consumption	750 µA***	55 µA	116 µA	110 µA	N.A.	53 µA	25 µA	4.3 µA	36 µA	120 µA
PSRR	127 dB@DC	74 dB@DC	68 dB@100Hz	83 dB	N.A.	N.A.	70 dB@10kHz	84 dB@10Hz	84 dB@DC	30 dB@100kHz
Number of Temp Trims	1	1	2	2	1	4	4	1	2	0
Temperature Drift (±) 3 Sigma Estimates	3 ppm/°C	9 ppm/°C**	6 ppm/°C*	5 ppm/°C*	5 ppm/°C	2 ppm/°C	5 ppm/°C**	10 ppm/°C**	4 ppm/°C**	12 ppm/°C**

* Sample population information not available, drifts are maximum measured.
** 3 sigma (±) ppm drift calculated from sample population information provided in work.
*** The current consumption of the continuous time bandgap reference is 4 µA. If the precision bandgap reference is active 1% of the time the average current consumption is reduced to 12 µA. 12 µA is an estimation calculated by adding the current consumption of the continuous time bandgap reference to the current consumption of the precision bandgap reference multiplied by 0.01.

continuous time bandgap reference, the V_{be} generator circuit and the V_{ref} generator circuit.

VI. CONCLUSIONS

A precision fully differential switched capacitor bandgap reference has been shown to achieve ±3 ppm/°C temperature drift from -40 °C to 110 °C. In an application where reference voltage precision is critical, a single temperature trim option for obtaining precision has been presented. A fully differential switched capacitor implementation removes many of the most significant error sources found in the continuous time counterparts. A scheme for sampling the V_{be} term of V_{ref} directly onto the output of the differential amplifier was presented that avoids an error source otherwise introduced with standard capacitor multiplication. A technique for bandwidth matching the differential amplifier in both phases of operation was also presented to further improve accuracy by enabling the use of minimum sized switches connected to the critical charge conservation nodes of the amplifier.

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Bradford L. Hunter (M'15) received his B.Sc. degree and M. Sc. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, Georgia, in The United States in 2003 and 2004 respectively.

From 2004 to 2006 he was employed by Freescale Semiconductor designing high speed SRAMs. From 2006 to 2008 he was employed by IBM Microelectronics designing analog cores for ASIC products. In 2008 he joined Texas Instruments designing analog integrated circuit catalog products for battery management applications. He is currently a Senior Member of Technical Staff and resides in Austin, Texas at the Unitrode Design Center. His primary areas of interest of design include analog to digital converters, linear and switched mode regulators, and high voltage circuits up to 120 V. He is the inventor on over 15 US patents in the area of integrated circuits.

Wallace E. (Ed) Matthews (M'81) received the B.Sc. degree in electrical engineering from Mississippi State University, Starkville, Mississippi in the United States in 1981 and the M.Sc. degree in electrical engineering from the University of California, Berkeley, California in the United States in 1982.

He worked for several companies from 1982 to 1990 developing precision CMOS data converters. He joined the staff of Benchmarq Microelectronics in 1990 where he helped pioneer the field of battery management integrated circuits by serving in various technical and management roles, including vice-president and chief engineer. In 1996 he helped lead Benchmarq to a successful IPO. The company later merged with Unitrode before being acquired by Texas Instruments. He currently resides in Austin, Texas where he manages the Austin Design Center battery gauge design team. His research interests are in sub-microvolt signal acquisition and data conversion. He was elected TI-Fellow in 1999, holds numerous circuit and system level patents in the field of battery management and has authored refereed papers and conference presentations.